Methods for eliminating the limit cycle oscillation due to low resolution ADC/DPWM in digitally controlled DC-DC converters

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in partial fulfilment for the degree of

Doctor of Philosophy

by

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CERTIFICATE

This is to certify that the thesis titled **Methods for eliminating the limit cycle oscillation due to low resolution ADC/DPWM in digitally controlled DC-DC converters,** submitted by **Sajitha G.**, to the Indian Institute of Space Science and Technology, Thiruvananthapuram, for the award of the degree of **Doctor of Philosophy**, is a bona fide record of the research work done by her under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Place : Thiruvananthapuram
Date : January, 2018

DECLARATION

I declare that this thesis titled **Methods for eliminating the limit cycle oscillation due to low resolution ADC/DPWM in digitally controlled DC-DC converters** submitted in fulfilment of the Degree of Doctor of Philosophy is a record of original work carried out by me under the supervision of **Dr. Thomas Kurian**, and has not formed the basis for the award of any degree, diploma, associate ship, fellowship or other titles in this or any other Institution or University of higher learning. In keeping with the ethical practice in reporting scientific information, due acknowledgments have been made wherever the findings of others have been cited.

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SC11D006

Place : Thiruvananthapuram
Date : January, 2018

In loving memory of my mother

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ABSTRACT

Digital controllers have become an attractive choice in DC-DC converter as they have a number of potential advantages which include lower sensitivity to parameter variations, programmability, improvement in dynamic response by incorporating advanced control algorithm, auto tuning and communication capability. Most of the digital controllers are based on conventional architectures where Analog to Digital Converters (ADC) are used to digitize the converter state variables. A digital control algorithm estimates the duty cycle, which is given to a Digital Pulse Width Modulator (DPWM) to generate the Pulse Width Modulated (PWM) waveform. To achieve better regulation of the output voltage, a high speed and high resolution ADC is required to sample the output voltage at PWM switching frequency. Furthermore, the resolution of DPWM should be greater than that of the ADC to avoid undesirable quantization effects such as limit cycle oscillation. The design platforms for the digital controller are FPGAs, ASICs and DSP Processors. But there are practical limitations to the implementation of a power and area efficient ASIC. Hence, different methods to realize high speed, high resolution ADC and DPWM have been reported. But all the earlier reported work has its own drawback. However, no detailed studies are reported that implements a digital controller with low resolution ADC and DPWM as it may lead to limit cycle oscillation.

In the thesis, investigation was carried out to reduce the limit cycle oscillation due to low resolution ADC and DPWM. Thus the thesis primarily focuses on a reduced state, computationally efficient Kalman filter for reducing the limit cycle oscillation due to low resolution ADC. The thesis also focuses on a scheme to use low resolution DPWM with no limit cycle oscillation. Significant attempts were made to improve the conducted emissions from the converter, apart from improving the effective resolution.

The contribution of the thesis is summarized as given below.

I) A reduced state Kalman filter is proposed to reduce the limit cycle oscillations caused by low resolution ADCs in digitally controlled DC-

DC converter. The reduction in state of the converter has facilitated the minimization of the clock cycle required for computation. This has been achieved by reducing the vector states of converter to scalar state with Kalman gain computed offline.

II) A novel method for the reduction in limit cycle oscillation due to low resolution DPWM by combining the advantages of sigma delta modulation scheme and frequency modulation of switching frequency has been proposed. In this work, the correction of quantization error due to low resolution DPWM is accomplished by changing the switching frequency. The error due to the quantization of DPWM is accumulated for few clock cycles and the switching frequency is adjusted in the last cycle such that the duty ratio changes by the number of LSBs corresponding to the quantization error. The quantization error correction increases the effective resolution of DPWM thereby reducing the ripple due to limit cycle oscillations. Further, it also reduces the conducted electromagnetic emissions.

III) A most appropriate design for the digital controller by using low resolution ADC (6-bit) and DPWM (7-bit) by combining the reduced state Kalman filter and quantization error correction has been proposed. The reduced state Kalman filter gives the optimal output voltage from the noisy measurement from low resolution ADC and the quantization error correction increases the effective resolution of DPWM.

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ABBREVIATIONS

IIST	Indian Institute of Space Science and Technology
VSSC	Vikram Sarabhai Space Centre
PWM	Pulse Width Modulation
ADC	Analog to Digital Converter
DPWM	Digital Pulse Width Modulator
FPGA	Field Programmable Gate Array
ASIC	Application Specific Integrated Circuit
DSP	Digital Signal Processing
SMPS	Switched Mode Power Supply
EMI	Electromagnetic Interference
PID	Proportional Integral Derivative
CCM	Continuous Conduction Mode
PRBS	Pseudo Random Binary Signal
DCM	Discontinuous Conduction Mode
MIMO	Multi Input Multi Output
PI	Proportional Integral
FM	Frequency Modulation
RCF	Random Carrier Frequency
CFM	Carrier Frequency Modulation
RCFM	Random Carrier Frequency Modulation
PCFM	Periodic Carrier Frequency Modulation
RPPM	Random Pulse Position Modulation
RPWM	Random Pulse Width Modulation
BF-PT	Bi-Frequency Pulse Train
PCM-BF	Peak Current Mode Bi-Frequency control
BF-DPWM	Bi-Frequency DPWM
QEC	Quantization Error Correction
MUX	Multiplexer
POR	Power On Reset
MMSE	Minimum Mean Square Error
PLL	Phase Locked Loop
MAC	Multiply and Accumulate
MPY	Multiply the product of two registers with accumulator
MUL	Multiply
VCO	Voltage Controlled Oscillator
UART	Universal Asynchronous Receiver/Transmitter
SPI	Serial Peripheral Interface Bus
I^2C	Inter-Integrated Circuit

CHAPTER 1

Introduction

A DC-DC converter is a circuit that converts an unregulated DC input to a regulated DC output at a desired voltage level. They provide a regulated output voltage that remains stable independent of the variation in the input voltage, load current, temperature and time. DC-DC converters are employed in a variety of applications, including power supplies for personal computers, office equipment, spacecraft power systems, telecommunications equipment and DC motor drives. In aerospace applications, these are used extensively to power the various Avionics packages from raw unregulated battery.

This chapter briefly describes the background and motivation of the thesis and gives an outline of the chapters that follow. The overview of switched mode DC-DC converters are briefly reviewed in Section 1.1. The operating principle of buck converter is given in Section 1.2. The standard analog control architecture for switched mode DC-DC converters is presented in Section 1.3. Benefits of digital control in switched mode DC-DC converters are discussed in Section 1.3. An outline of the thesis is given in Section 1.4.

1.1 Overview of switched mode DC- DC converters

There are two types of DC-DC converter namely linear regulators and switched mode power supplies. The linear regulators operate the power transistors in the linear mode. The limitations of the linear regulator are that they are not energy efficient, require bulky heat sink and can only step down the voltage level. In contrast to linear regulators, switched mode DC-DC converters use power semiconductor devices in either the on state or the off state and are highly efficient.

A switched mode DC-DC converter consist of two stages namely power stage and the control stage. The power stage makes the energy conversion while the control stage controls power switches to obtain the desired regulated output voltage.

The output regulation is achieved by Pulse Width Modulation (PWM), where the power switch is commuted at a constant frequency but varying duty cycle. Based on the power stage, switched mode DC-DC converter can be broadly classified into isolated and non-isolated topology. Four commonly used topologies for non-isolated switched mode DC-DC converter are expressed in terms of conversion ratio and are illustrated in Figure 1.1.

For a DC-DC converter, the conversion ratio is defined as the ratio of output voltage, V_0, to input voltage, V_s, and is given as

$$\mathrm{M(D)} = \frac{\mathrm{V_o}}{\mathrm{V_s}} \tag{1.1}$$

A brief description of the four topologies is presented below:

1) Buck Converter*:* This topology derives a low voltage from the input DC voltage and has conversion ratio $\mathrm{M(D)} = \mathrm{D}$, where D is the duty ratio.

2) Boost Converter*:* In this topology the positions of the switch and inductor are interchanged. This converter produces an output voltage that is greater in magnitude than the input voltage. Its conversion ratio is given by, $\mathrm{M(D)} = \frac{1}{1-\mathrm{D}}$.

3) Buck-Boost Converter*:* In the buck-boost converter, the switch alternately connects the inductor across the power input and output voltages. This converter inverts the polarity of the voltage, and can either increase or decrease the voltage magnitude. The conversion ratio is given by, $\mathrm{M(D)} = \frac{\mathrm{D}}{1-\mathrm{D}}$.

4) Cuk Converter*:* The Cuk converter contains inductors in series with the converter input and output ports. The switch network alternately connects a capacitor to the input and output inductors. The conversion ratio is identical to that of the buck-boost converter. Hence, this converter also inverts the voltage polarity and can either increase or decrease the voltage magnitude. This has lower ripple compared to buck-boost.

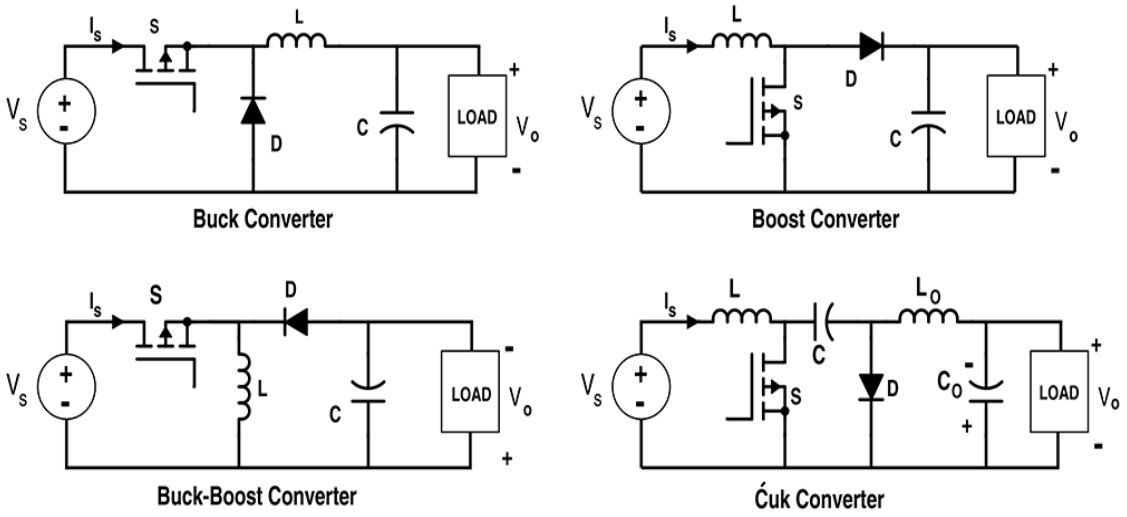

Figure 1.1: Basic non-isolated converter topologies

In the above topologies, the switch is realized using a power MOSFET or BJT. However, in most of the practical applications, isolation is required for the DC-DC converters. The most widely used isolated topologies are the flyback, forward, push-pull, half-bridge and full-bridge converters. The details of the isolated topologies are not dealt as the thesis basically uses the buck topology for the research.

1.2 Operating principle of buck converter

The configuration of buck converter is given in Figure 1.2. V_{in} is the input voltage, which can be supplied by batteries, DC bus, or other DC voltage sources. The switch that is connected between the input source and the inductor L is called the "main switch" (S1) and is usually implemented with a power MOSFET. The other switch is connected between the inductor L and the ground terminal. It can be implemented with either a power MOSFET (synchronous rectifier, S2) or a free-wheeling diode (asynchronous rectifier). S1 and S2 turn on alternatively within each switching period T_s, with a switching frequency, $f_{sw} = 1/T_s$. The common node in between the S1, S2 switches and inductor L is called the switching node, which is denoted as V_x.

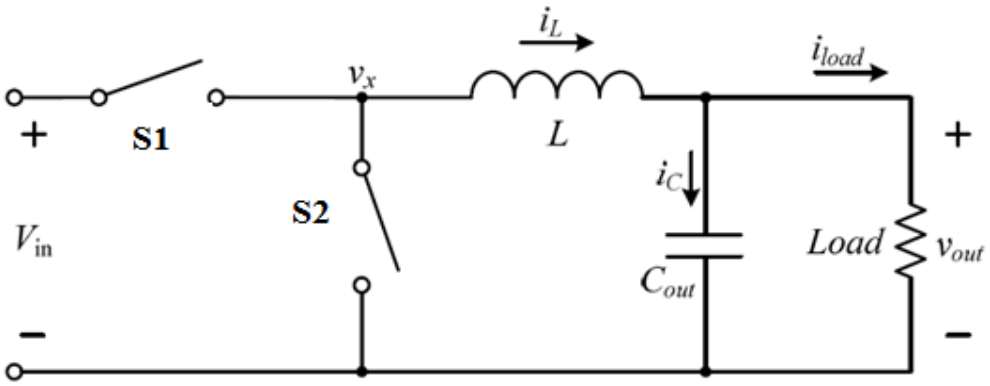

Figure 1.2: Configuration of buck converter [74]

Basic steady state voltage and current waveforms of a conventional buck converter under Continuous Conduction Mode (CCM) are as shown in Figure 1.3. Within each switching period T_s, the percentage of time when the switch S1 is on, while S2 is off is denoted as the duty cycle D. On the other hand, the percentage of time when S1 is off, while S2 is on is generally denoted as D' or $1 - D$. When the S1 switch is on, the switching node V_x is pulled to V_{in}. The voltage across the inductor is $V_{in} - V_{out}$ and the current $i_L(t)$ in the inductor ramps up with a slew rate of k_D, where $k_D = \frac{Vin-Vout}{L}$. When S1 is off, the switching node V_x is pulled to ground. The current $i_L(t)$ in the inductor ramps down with a slew rate of $k_{D'}$, where $k_{D'} = \frac{-Vout}{L}$. The ripple current of the inductor, Δi_L, is defined as the peak to peak variation of $i_L(t)$, which is determined by (1.2)

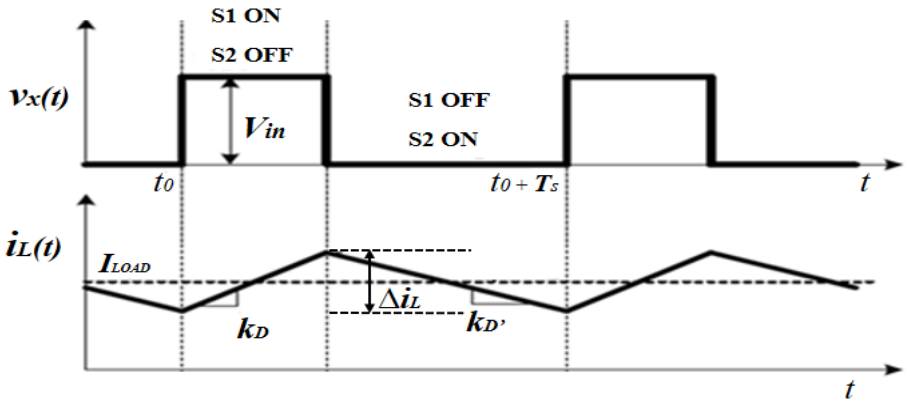

Figure 1.3: Steady State waveforms of buck converter in CCM [74]

$$\Delta i_L = K_D D T_s = \frac{(V_{in} - V_{out}) D T_s}{L} = \frac{(V_{in} - V_{out}) D}{L f_s} \quad (1.2)$$

A good estimate on the ripple current of the inductor is 10 % of the maximum load current. In order to operate the buck converter in CCM, the value of the inductor should be equal to or greater than

$$L = \frac{V_{out}\,(V_{in} - V_{out})}{\Delta i_L f_s V_{in}} \quad (1.3)$$

The maximum current through the main switch is given by

$$I_{SW}(\max) = \frac{\Delta i_L}{2} + I_{load}(\max) \quad (1.4)$$

Under steady state, the value of the inductor current is the same at the beginning and end of the each switching cycle. This phenomenon is called “inductor voltage second balance”. Based on this the relationship between the input voltage and output voltage is given by

$$K_D D T_s = K_{D'} D' T_s \quad (1.5)$$

$$\frac{(V_{in} - V_{out}) D T_s}{L} = \frac{V_{out} D' T_s}{L} \quad (1.6)$$

$$V_{out} = V_{in} D \quad (1.7)$$

The output capacitor is selected based on the ripple voltage, ΔV_{out}, and is given by

$$C_{out}(\min) = \frac{\Delta i_L}{8 f_s \Delta V_{out}} \quad (1.8)$$

In a DC-DC converter application, it is desired to obtain a constant output voltage in spite of disturbances in input voltage and load current. A negative feedback for control is used that automatically adjusts the duty cycle as needed to obtain the desired output voltage with high accuracy, regardless of variation in input and load. The traditional approach for controllers of DC-DC converters is based on duty ratio adjustment and uses analog implementation schemes. A block diagram of a DC-DC converter with analog feedback system is shown in Figure 1.4. The output voltage is scaled down with the transfer function, $H(s)$. The scaled down output voltage is compared with a stable voltage reference, v_{ref}. The error between the scaled down

output voltage and the reference is given to a compensator and it makes the output voltage regulated around reference voltage. The output of the compensator is compared with a ramp to generate the PWM signal that drives the gate of the MOSFET. Analog control techniques offer robust control, but suffer from serious limitations such as sensitivity to noise and temperature change. But over the past number of years, digitally controlled techniques have received increased research attention. Hence this thesis deals with digitally controlled DC-DC Converter.

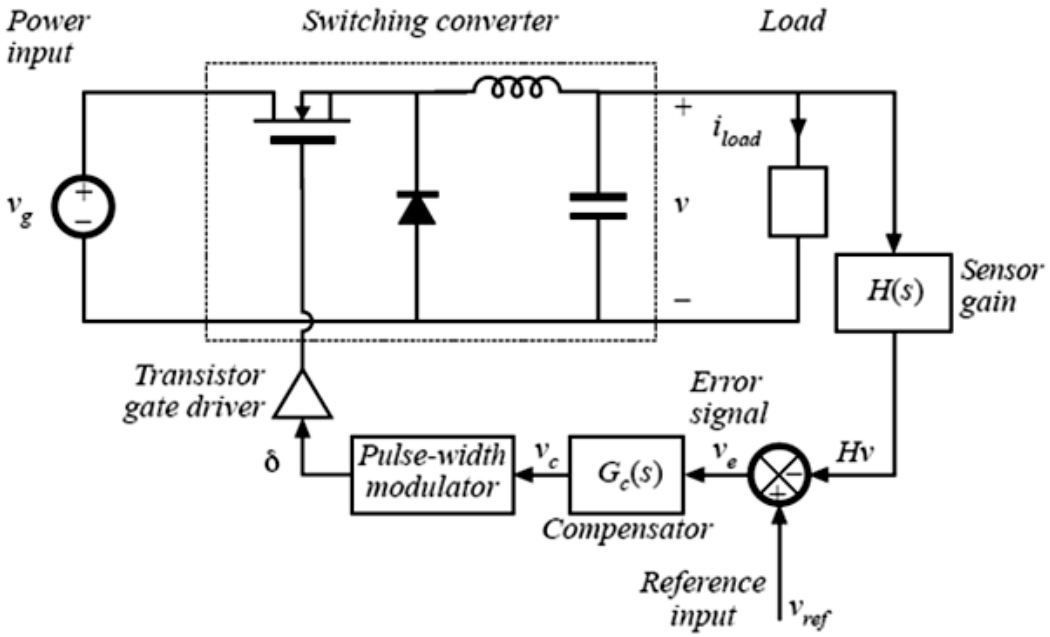

Figure 1.4: Block diagram of buck DC- DC converter using analog controller [75]

1.3 Digital controllers for DC- DC converters

Digital control of high frequency DC-DC converter has been shown to provide many possible benefits, including improved immunity to noise and parameter variations, reduction in the number of external components, real time programmability, ability to implement sophisticated control schemes and integration of advanced features such as adaptive tuning, system diagnosis and health monitoring. Switching power converters are powerful sources of Electro Magnetic Interferences (EMI) because of the large di/dt and dv/dt. EMI mitigation techniques can be easily incorporated in digitally controlled DC-DC converter.

Most of the digital controllers are based on conventional architectures where ADCs are used to digitize the converter state variables and a digital control algorithm determines the duty cycle, which drives the DPWM. Figure 1.5 shows the block diagram of a digitally controlled PWM DC-DC converter. In a digitally controlled DC-DC converter, the sensed output voltage is digitized using ADC and is then compared with the reference signal. The error signal, which is the difference between the output of ADC and the reference signal is given to a digital compensator. The discrete time compensator computes the digital duty cycle command and a DPWM outputs the gate drive pulses at the desired switching frequency based on the digital duty cycle command.

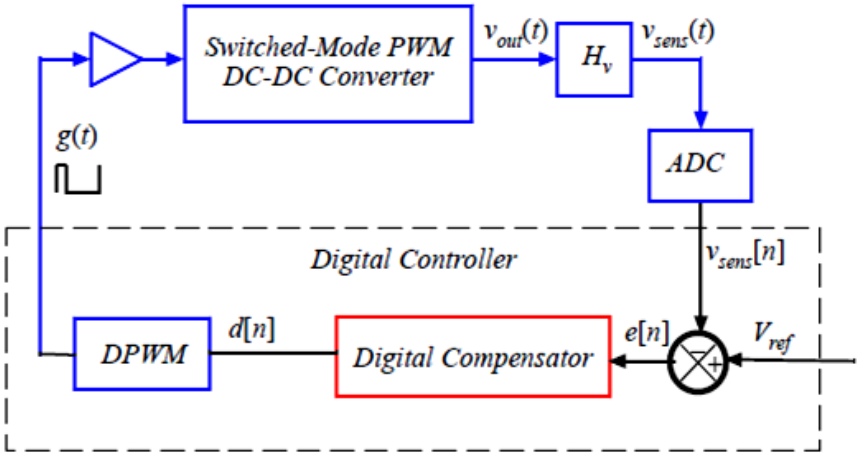

Figure 1.5: Block diagram of digitally controlled DC-DC converter

Although much research is being carried out in this field, there are many limitations to the practical implementation of digitally controlled DC-DC converter. Normally, analog control provides fine resolution of output voltages, which is only limited by the loop gain and noise levels. However, a digital controller has a finite set of discrete levels due to the quantization of ADC and the DPWM in the digital control loop. Thus the quantization of ADC and DPWM is critical to both the static and dynamic performance of the DC- DC Converter. In order to achieve tight regulation of the output voltage, a high resolution ADC is required. Also the ADC should be sampled at the rate equal to the switching frequency. ADCs with low latency are desirable, since the latency causes a phase shift into the loop that may degrade the system response.

Moreover, to get finer control of duty cycle, a high resolution, high frequency DPWM is required. The discrete set of duty ratios and ultimately the discrete set of achievable output voltages depend on the resolution of DPWM. If the DPWM resolution is not sufficiently high, an undesirable limit cycle oscillation can occur. In limit cycle oscillations, the output goes into an oscillation of fixed amplitude and frequency. Steady state limit cycle may be undesirable if it leads to a large ripple in output voltage. Furthermore, since the limit cycle amplitude and frequency are hard to predict, it is difficult to analyze and compensate for the output noise and the EMI produced by the converter.

1.4 Motivation

Based on the explanation provided in the previous section, it is clear that digital controller has limitations when compared to analog controller for power converters. A complete analog system is simpler than implementing high speed, high resolution ADC and DPWM. Moreover, in digital control, the control algorithms have to be realized by software in DSP or FPGA/ASIC in fixed point algorithmic calculation. Thus the ASIC implementations should invariably integrate fast, high resolution ADC and DPWM apart from the digital control hardware which results in increase of overall area and power consumption. Accuracy comparable to analog controllers is achieved only by means of sufficient bit resolution and/or dedicated signal processing provisions. Hence the design of ASIC, for digital control, with analog like performances in terms of dynamic capabilities, area and power consumption is still a challenging issue.

Hence the motivation of this thesis is to simplify the requirements on the resolution of ADC and DPWM in high frequency digitally controlled DC-DC converter through suitable signal processing methods without sacrificing output accuracy. While simplifying the requirements of ADC and DPWM it is very essential that the performance of the converter should not be affected. It is evident that low resolution ADC and DPWM will cause limit cycle oscillations. Hence studies are carried out to reduce the limit cycle oscillation caused by low resolution ADC, DPWM and to arrive at the most appropriate configuration for high frequency digitally controlled DC-DC converter.

1.5 Thesis overview

Chapter 2 gives an overview of the research work carried out in the area of digitally controlled DC-DC converter. The literature survey includes the different architectures of ADC, DPWM, control schemes and EMI mitigation schemes.

The main goal of this thesis is to explore methods to reduce the limit cycle oscillation caused by low resolution ADC and DPWM in digitally controlled DC-DC converter. The research work presented in the thesis consists of three parts. In the first part, a reduced state Kalman filter is proposed to reduce the limit cycle oscillations caused by low resolution ADCs in digitally controlled DC-DC Converter. The reduction in the vector state of the converter to scalar state has facilitated the minimization of the clock cycle required for computation. Moreover, the Kalman gain has been computed offline thereby reducing the computation time.

Chapter 3 focuses on the proposed reduced state Kalman filter and how the vector state of the converter has been reduced to scalar state. The offline computation of the Kalman gain is also given. The modeling of the converter with the reduced state Kalman filter, using MATLAB, is also presented. The simulation results are also presented. The scheme was practically implemented and the design using DSP processor is also presented. An experimental prototype is built using surface mount devices and the results are explained.

In the second part of the thesis, a method for the reduction in limit cycle oscillation due to low resolution DPWM by combining the advantages of sigma delta modulation scheme and frequency modulation of switching frequency is carried out. In this work, the correction of quantization error due to low resolution DPWM is accomplished by changing the switching frequency. The error due to the quantization of DPWM was accumulated for few clock cycles and the switching frequency was adjusted in the last cycle such that the duty ratio changes by the number of LSBs corresponding to the quantization error. The quantization error correction increases the effective resolution of DPWM thereby reducing the ripple due to limit cycle oscillation.

Chapter 4 focuses on the proposed scheme that increases the effective resolution of DPWM thereby reducing the limit cycle oscillation by adjusting the switching frequency. The modeling of the converter, using MATLAB, and the simulation results are also presented. Further the design and implementation using DSP processor is presented.

In the third part of the thesis, both the above mentioned schemes are combined to achieve better performance with low resolution ADC and DPWM. The most appropriate configuration of the digitally controlled DC-DC converter with low resolution ADC and DPWM is presented in chapter 5. The simulation and experimental results are also presented.

Finally, in Chapter 6, the conclusion and future scope of the research topics is presented.

CHAPTER 2

Literature Survey

This chapter gives a survey of the research work carried out in the area of digitally controlled DC-DC converter. As mentioned earlier, to achieve tight regulation and to avoid limit cycle oscillation, a high resolution ADC and DPWM is required. As this thesis mainly aims at the elimination of limit cycle oscillation due to low resolution ADC and DPWM, the analysis so far carried out and the conditions required to avoid limit cycle is presented in Section 2.1. No significant attempt was so far made to realize digitally controlled DC-DC converter with low resolution ADC and DPWM. Meanwhile, in the area of digitally controlled DC-DC converter extensive research has been carried out on different schemes of high resolution ADC, control law and high resolution DPWM architectures. The research so far carried out in digitally controlled DC-DC converter is presented in the subsequent sections. An overview of the advances in digital control of low to medium DC-DC switching converters is given in [5]. The already demonstrated and forthcoming impact of digital control in high frequency power electronics is given in [6]. The research carried out on different schemes of high resolution ADC and DPWM architectures and the tradeoffs among resolution, silicon area and power consumption for these architectures are presented in Section 2.2 and Section 2.3. Software methods have been reported to increase the resolution of DPWM and it is also given in Section 2.3. A survey of various control laws reported in literature is presented in Section 2.4. As the thesis also aims at reducing the conducted electromagnetic emissions, the research work so far carried out in the area of EMI mitigation techniques by the modulation of switching frequency is also given in Section 2.5.

2.1 Limit cycle oscillation

Limit cycles may result from the presence of signal amplitude quantizers like the ADC and DPWM modules in the feedback loop [3] [4] [70]. Steady state

limit cycling may be undesirable if it leads to large amplitude (or unpredicted) output voltage variation. If the resolution of ADC is n_{adc} and that of DPWM is n_{dpwm}, then the quantization step for ADC is given by $\Delta V_{adc} = \frac{V_m}{2^{n_{adc}}}$ and for DPWM is given by $\Delta V_{dpwm} = \frac{V_m}{2^{n_{dpwm}}}$, where, V_m is the voltage range of the ADC and DPWM. Let us assume that the resolution of DPWM is less than ADC. Then there is no DPWM level that maps into the ADC bin corresponding to the reference voltage (this ADC bin will be referred to as the zero error bin). In steady state, the controller will be attempting to drive to the zero error bin, however due to the lack of a DPWM level, it will alternate between the DPWM levels around the zero error bin. This results in the non-equilibrium behavior, such as steady state limit cycling.

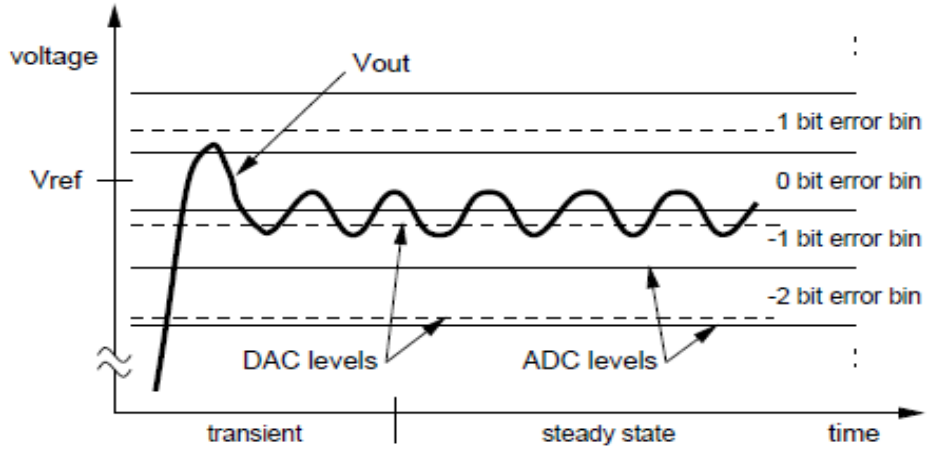

Figure 2.1: Qualitative behavior of output voltage (V_{out}) for DPWM resolution less than ADC [3]

Thus the first step towards eliminating limit cycles is to ensure that under all circumstances there is a DPWM level that maps into the zero error bin. This can be guaranteed if the resolution of the DPWM is finer than the resolution of the ADC. A one bit difference in the resolutions, $n_{dpwm=}n_{adc} + 1$, seems sufficient in most applications since it provides two DPWM levels per one ADC level.

No Limit Cycle Condition # 1

$$\mathbf{resolution(DPWM) > resolution(ADC)} \qquad (2.1)$$

In a digitally controlled DC-DC converter, the minimum required resolution of the ADC to satisfy the specification for the output voltage regulation is given by

$$n_{adc} = \text{int}\left[\log_2 \frac{V_{max} V_{out}}{V_{ref} \Delta V_{out}}\right] \tag{2.2}$$

where, V_{max} is the full range voltage of the ADC assuming unipolar operation in the range 0 V to V_{max}. V_{ref} is the reference voltage and V_{out} is the output voltage. ΔV_{out} is the allowed variation in output voltage. int[ ] indicate that the upper rounded integer argument of the value is taken.

Even if the above condition is met, limit cycling may still occur if the feed forward term is not perfect and the control law has no integral term. In this case, the controller relies on non-zero error signal to drive V_{out} towards the zero error bin. However, once V_{out} is in the zero error bin, the error signal becomes zero, and V_{out} drops back below the zero error bin. This sequence repeats, resulting in steady state limit cycling. This problem can be solved by the inclusion of an integral term in the control law.

No Limit Cycle Condition # 2

$$\mathbf{0 < K_i \leqslant 1} \tag{2.3}$$

where K_i is the integral gain. The two conditions suggested above are not sufficient for the elimination of steady state limit cycles, since the non-linearity of the quantizers in the feedback loop may still cause limit cycling for high loop gains. Non-linear system analysis tools, such as describing functions can be used to determine the maximum allowable loop gain, which does not induce limit cycles. The describing function presented in [4] is given in Appendix 1. Normally to prevent limit cycle oscillation

$$\mathbf{1 + N(A)L(j\omega) \neq 0} \tag{2.4}$$

where $N(A)$ is the describing function of the quantizer and $L(j\omega)$ is the loop transmission from the output of the ADC to the input.

2.2 Architecture of ADC

Static and dynamic output voltage regulation capabilities of digitally controlled DC-DC converter depend on the characteristics of the ADC. Conventional high speed, high resolution ADCs consume power and chip area. Moreover, they require precision analog components. Further, topologies with low latency are desirable, since delays in the ADC correspond to phase delay that may degrade the loop response.

A wide choice of ADC architectures exist that differs in resolution, bandwidth, accuracy, and power requirements. The major ADC architectures are flash, successive approximation, and pipelined with multiple flash stages. Both successive approximation and pipelined ADC will introduce larger latency since they need several cycles to convert the analog signal. On the other side, the flash architecture has the advantage of being very fast because the conversion occurs in a single cycle. Therefore, the flash architecture is preferable for the design of digital controller. The main disadvantage of the flash structure is that it requires a large number of comparators (2^n-1 comparators for an n bit ADC). The 9-bits full range ADC will require 511 comparators, which require large core area and power consumption. Thus a high resolution ADC that covers the full range demands excessive power and silicon area.

A compromise solution used in [1] [2] [7] [8] [9] is a window based ADC architecture. It is based on the observation that under normal operation the output voltage V_o of a regulator will not deviate substantially from the reference voltage. Thus, the output voltage has to be quantized only over the regulation window around the reference signal, V_{ref}.

A block diagram of a flash implementation of such a “window” ADC is shown in Figure. 2.2. In this ADC, a number of comparators are connected to V_{ref} through an offset network with steps ΔV_{ref}, creating a few quantization bins around V_{ref}. Since the output voltage V_o is compared against V_{ref}, the resulting digital signal (D_e) is the difference between the two, which is a digital representation of the error signal V_e. Hence, it has the functionality of both an ADC and an error amplifier.

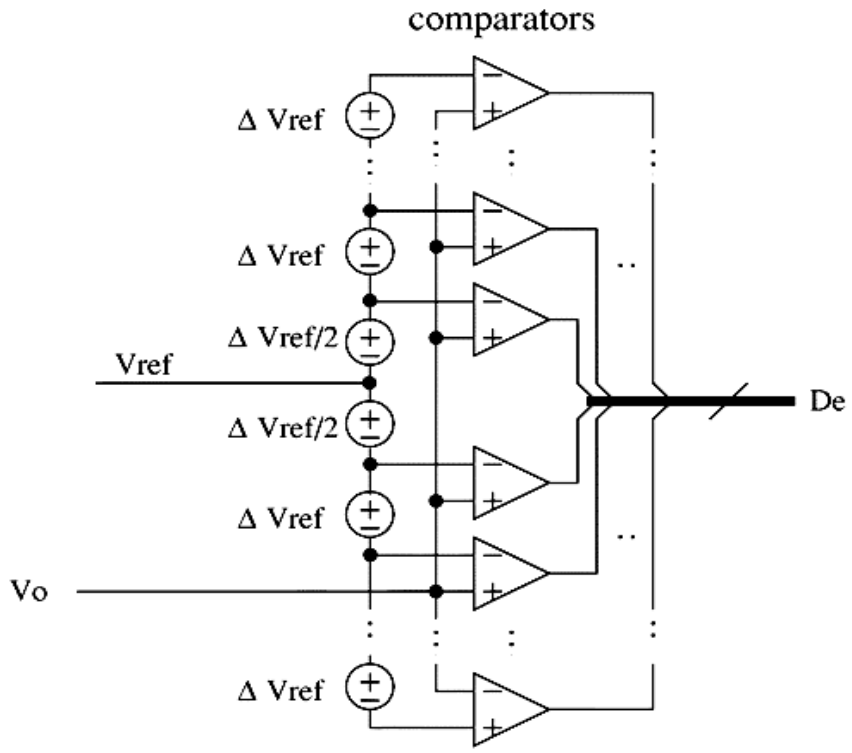

Figure 2.2: Flash window type ADC [1]

A number of variations in the windowed-flash architecture have been explored. In switching power supply, the sensed analog voltage comes from the output of a switching power converter. This signal has large switching noise, which can be a problem for many conventional ADC such as the basic flash configuration. The switching noise can produce undesirable aliasing effects in the quantization process. For example, typically the ADC is sampled at the converter switching frequency, and hence switching frequency noise could be aliased to a DC offset. To prevent aliasing effects and to provide accurate DC regulation, ADCs which average the input signal over each sampling period are desirable. The delay line ADC [2] has the unique advantage that it does not require any precision analog components, and that it can be implemented using standard logic gates. Figure 2.3 shows the basic delay line ADC configuration implemented in [2]. The delay line ADC is based on the principle that the propagation delay of a logic gate in a standard CMOS process increases if the gate supply voltage is reduced. If the analog input voltage (i.e. the sensed converter output voltage) is lower, the cell delay t_d is longer,

and the test pulse propagates to fewer taps along the delay line. To the first order, the propagation delay t_d as a function of the supply voltage V_{DD} is given by

$$t_d = K \frac{V_{DD}}{(V_{DD} - V_{th})^2} \tag{2.5}$$

where V_{th} is the MOS device threshold voltage and K is a constant that depends on device/process parameter and the capacitive loading of the gate.

For a higher sensed voltage, the cell delay is shorter and the test pulse propagates further along the delay line. To perform a conversion, at the beginning of a switching cycle, a test pulse is propagated through the delay line. A string of delay cells forms a delay line supplied from the sensed voltage $V_{DD} = V_{sense}$. After a fixed conversion time, the taps are sampled by the signal 'Sample', which is the clock of the D flip flop. The result at the output of the flip flops (signal q_1 to q_8) is passed to a digital encoder to produce the digital output signal e. The encoder is used to produce the output in the desired code. The digital output gives the digital error between the sensed voltage and the reference. In the delay line ADC design, the length of the delay line effectively determines the reference value V_{ref} around which the ADC conversion characteristic is centered. In practice, because of process and temperature variations, the reference value obtained by the basic delay line ADC configuration cannot be precisely controlled. Variations in the effective V_{ref} result in variations of the regulated output voltage and the power supply may fail to meet the specified static and dynamic voltage regulation.

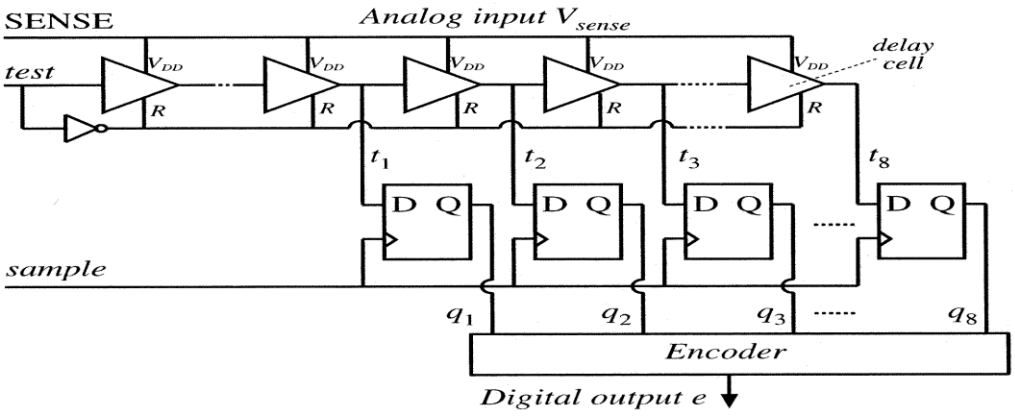

Figure 2.3: Basic delay line ADC [2]

An application specific delay line based windowed ADC with programmable reference, conversion time and accuracy of voltage is introduced in [7]. This work utilizes sigma delta DAC for the adjustment of reference and the ADC is fully implemented in a small silicon area. In [8] the non-uniform ADC quantizer parameters are selected to achieve good step load transient response. The input bins of the non-uniform ADC quantizer and the output quantization levels are selected to give improved dynamic performance without affecting the stability margins.

For very low power applications, the ADC has been implemented with a single comparator as presented in [9]. Minimally, the ADC conversion can be accomplished by a comparator, which decides whether the sensed output voltage is above or below a reference voltage. If the comparator is implemented as a dynamic comparator, which evaluates only upon command, it will not dissipate any power outside the brief evaluation period. In this single bit feedback case, a digital word representing the duty cycle is created by a counter, which counts up when the output is lower than the reference and counts down when the output is higher than the reference. This digital counter accomplishes the functionality of an integrator. There are certain disadvantages of using such a single bit feedback signal. First, the output will never reach an equilibrium voltage, rather it will approach a limit cycle, since the output is always measured to be in error (either too high or too low) and the error signal is not proportional to the magnitude of the error. Second, the response of the control loop must be slow in order to limit the magnitude of the steady state limit cycle. Thus this approach has poor transient performance, since excursions of the output voltage away from the reference voltage cannot be quantized appropriately.

The above discussion brings to light the fact that most of the previous work has been done in high resolution ADC or less effective low resolution ADC. The present work on the other hand focuses on the realization of a low resolution ADC with performance enhancement using signal processing techniques.

2.3 Architecture of DPWM

The DPWM module generates the duty cycle corresponding to a digital value. The design of the DPWM has been the subject of detailed study in the design of digitally controlled DC-DC converters [10-17] [69]. It has been shown, that in order to eliminate limit cycle at the output of a DC-DC converter, the resolution of the DPWM is critical [3], [4]. The resolution of DPWM must be better than the voltage resolution of the ADC in order for the DPWM to resolve to a voltage corresponding to zero steady state control error. Many novel schemes are available in literature to design a high resolution DPWM module for digital controller with moderate ADC resolution and high switching frequency, such as counter-comparator [10], delay line [9], hybrid DPWM [2], segmented ring DPWM [13], digital dither [3] and sigma delta modulator [14-16].

2.3.1 Hardware methods to implement high resolution DPWM

A survey and comparison of different architecture of DPWM in terms of high frequency capability, complexity, area, power consumption, sensitivity to process, temperature variations, linearity etc. are given in [5] [10].

2.3.1.1 Counter based DPWM

The simplest method to generate high resolution, high frequency DPWM is by using a fast clocked counter and a digital comparator [10] [11] as shown in Figure 2.4. This scheme is simple and easy to implement. In this scheme, a modulo N_r ($N_r = 2^N$) , where N is the resolution of DPWM) counter is used which is clocked at frequency,f_{clk}. A digital comparator outputs the PWM waveform by comparing the counter output with a latched digital control command,u[k]. A pulse is generated with duty cycle

$$d[k] = \frac{u[k]}{N_r} \tag{2.6}$$

The counter should be clocked at the period equal to the time resolution of the DPWM. The time resolution, $\Delta t_{DPWM} = \frac{T_s}{2^N}$, where T_s is the period of the switching waveform. Hence, to achieve N bit resolution at the switching frequency, f_{sw}, the

required clock frequency is $2^N x\, f_{sw}$. For example, an 8 bit resolution at the switching frequency of 1 MHz would require a clock frequency of 256 MHz. The system frequency becomes too high to be practical and can result in more difficult timing constraints. Hence the power consumption is high even though this scheme takes reasonable small die area.

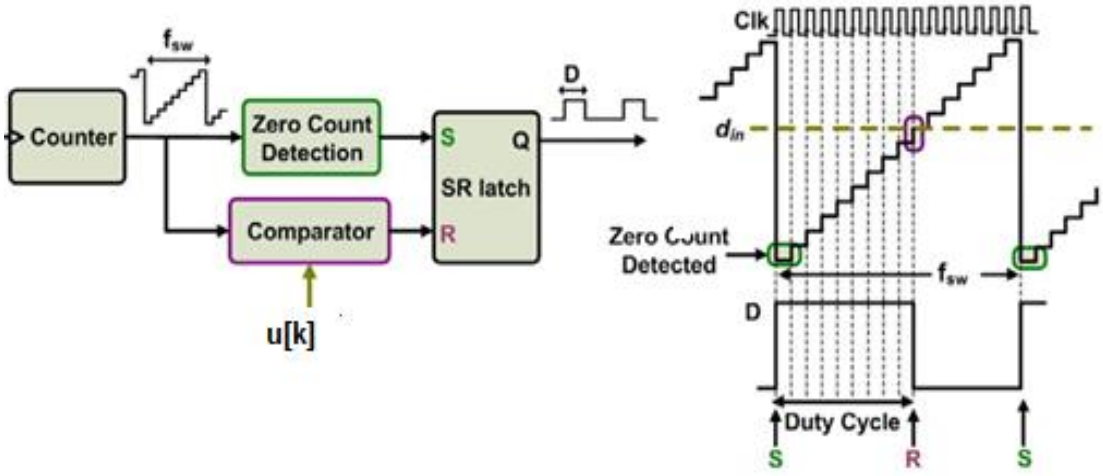

Figure 2.4: Counter based DPWM [69]

2.3.1.2 Delay line based DPWM

An architecture that circumvents the high frequency clock problem of the counter based DPWM is based on the tapped delay line [9]. Figure 2.5 shows delay line based DPWM. The essential components of a tapped delay line PWM circuit are the delay line and a multiplexer. 2^N delay elements and a $2^N{:}1$ multiplexer comprise the delay line based DPWM, where N is the DPWM resolution in bits. A pulse from a reference clock signal (frequency equal to the switching frequency) starts a cycle, and sets the PWM output to go high after a delay designed to match the propagation delay experienced through the multiplexer. The reference pulse propagates down the delay line, and when it reaches the output selected by the multiplexer, it is used to set the PWM output low. The total delay of the delay line is adjusted so that the total delay is equal to the reference clock period, $T_s = \frac{1}{f_{sw}}$. Each cell delay is equal to $\Delta t_{DPWM} = \frac{T_s}{2^N}$, where Δt_{DPWM} is the time resolution of DPWM. Since this approach uses the switching frequency clock, the power is

significantly reduced relative to the fast clocked counter approach. This approach is very power efficient, but requires significant implementation area, since the size of the multiplexer grows exponentially with the number of resolution bits. Also, if multiple PWM signals are needed, it requires the addition of multiplexers to single delay line. Another drawback of this scheme is that the cell delay changes with process and temperature variations.

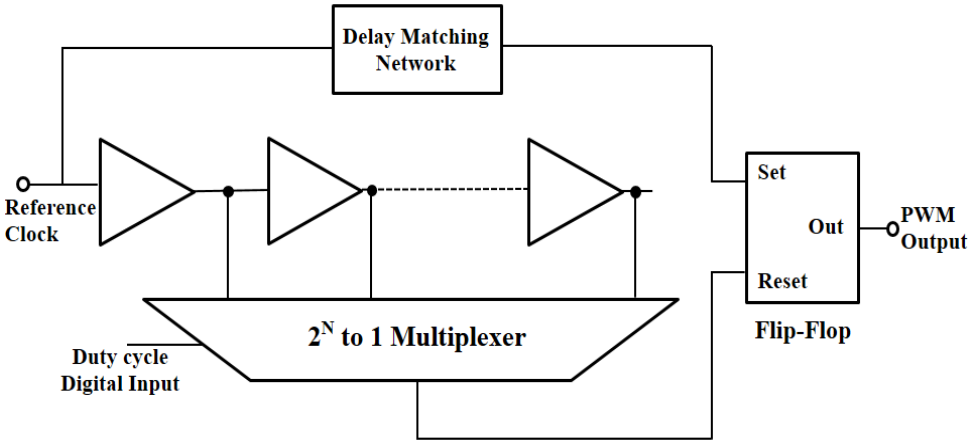

Figure 2.5: Delay line based DPWM [9]

2.3.1.3 Hybrid DPWM

To overcome the problems of counter based DPWM and delay line DPWM a hybrid delay line/counter scheme is proposed in [2] [11]. Figure 2.6 shows hybrid digital PWM with external clock. In this approach, an N-bit resolution is achieved using a N_c bit counter ($N_c < N$), whereas the remaining $N_d = N - N_c$ bits of resolution are obtained from a tapped delay line. The latched control word having N bits is split into the least significant N_d long U_{LSB} and N_c long the most significant bit, U_{MSB}. The clock frequency of the counter is given by $f_{clk} = 2^{N_c} x\, f_{sw}$, and the duty cycle of the output pulse is given by

$$d[k] = (U_{MSB} + \frac{U_{LSB}}{2^{N_d}}) \frac{T_{clk}}{T_s} \tag{2.7}$$

where T_{clk} is the period of the counter. Hybrid counter with delay line approach seems to reach a good compromise between area, clock frequency and resolution.

However, even this approach reaches a practical limit in terms of area and clock frequency as the underlying resolution is increased. In this scheme, in order to avoid DPWM non-linearity, care must be taken to ensure that the maximum delay of the tapped delay line is approximately matched with the delay associated with the counter's LSB.

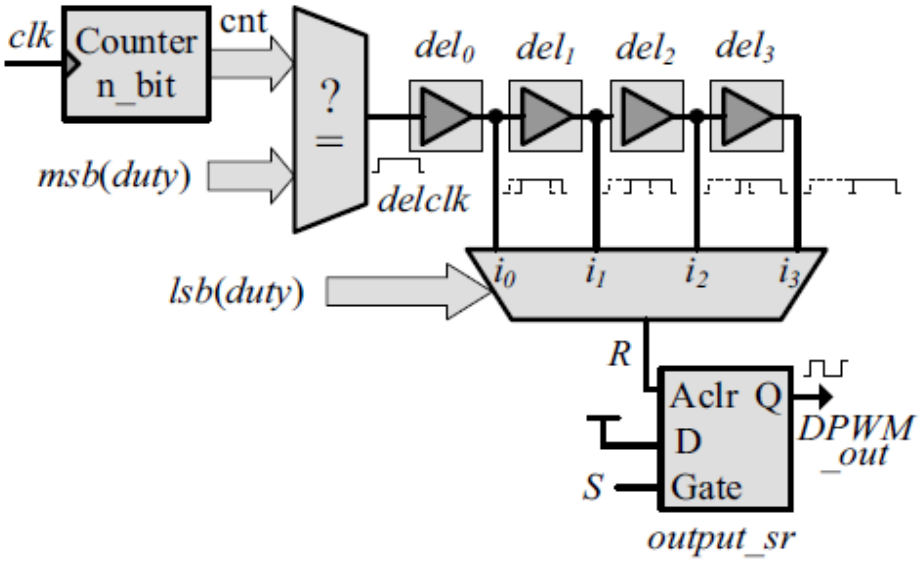

Figure 2.6: Hybrid DPWM with external clock [11]

To address this issue, a hybrid DPWM is proposed in [11], which utilizes a tapped delay line consisting of adjustable delay cells. The cell delays are continuously monitored and adjusted by a delay locked loop (DLL), ensuring that the tapped delay line yields constant delays, regardless of external factors. A new hybrid DPWM is implemented in [12] wherein the delay locked loop is implemented taking advantages of FPGA's advanced characteristics.

2.3.1.4 Ring oscillator MUX implementation of DPWM

In the delay line based DPWM and hybrid digital DPWM scheme presented above, the clock frequency which is equal to the switching frequency is given externally. As the total delay varies with temperature and process, the executed duty cycle is not always the same as the duty cycle command. As an alternative, the delay line itself is used in the form of ring oscillator which generates the clock at the switching frequency. In this case the process/temperature variations cause a drift in

switching frequency rather than the duty cycle. A ring oscillator Multiplexer (MUX) implementation of a DPWM module presented in [1] and illustrated in Figure 2.6 has area and power considerations similar to those of the delay line approach. However, this scheme has the advantage of a symmetric structure.

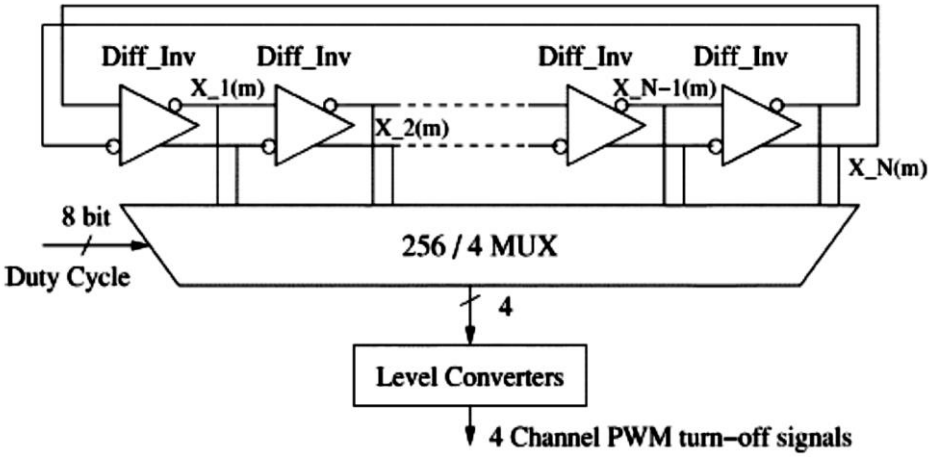

Figure 2.7: A ring oscillator MUX implementation of DPWM [1]

2.3.1.5 Segmented delay line DPWM

Segmented delay line architecture is a fragmented version of the delay line which, ultimately, will result in a smaller area compared to the delay line based DPWM [13]. Unlike the delay line architecture, where the DPWM resolution (N) requires 2^N delay elements forming one line and one 2^N: 1 multiplexer, the N bits can be segmented into groups of smaller delay lines (N_{seg}) with a smaller multiplexer for each line instead of one big multiplexer. A 6 bit DPWM (N = 6) can be segmented to three numbers of two bit delay lines (N_{seg}= 2), each has 4 delay elements ($2^{N_{seg}} = 2^2 = 4$) and a 4: 1 multiplexer as shown in Figure 2.8. The 4:1 multiplexer is controlled by two bits of d[n]. The delay in each of the four elements of the i^{th} segment is given by

$$\Delta t_i = 4\Delta t_{i-1} = 2^{2i}\Delta t_o \qquad (2.8)$$

The Δt_i delays are created by replicating the Δt_o delay cells. Thus this architecture will result in a smaller area compared to the delay line based DPWM that will need ($2^N = 2^6 = 64$) delay elements and one 64: 1 multiplexer [13].

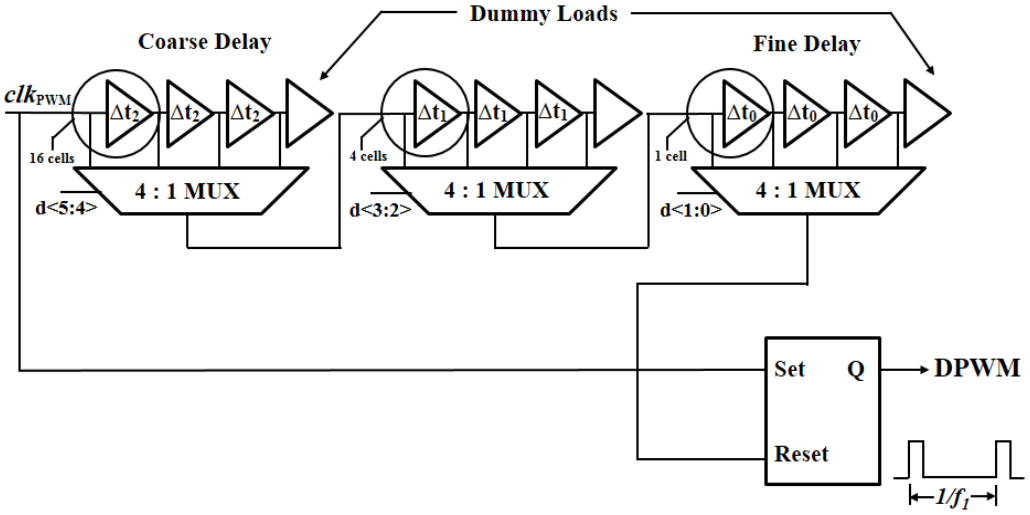

Figure 2.8: Segmented 6 bit DPWM [13]

2.3.2 Software methods to implement high resolution DPWM

Soft method such as dithering and sigma delta modulation scheme increases the effective resolution of a DPWM module without increasing the hardware resolution.

2.3.2.1 Dithering

A soft method known as dithering, as shown in Figure 2.9, to increase the effective resolution of a DPWM module without increasing the hardware resolution is proposed in [3]. The dither method involves applying a pattern to successive DPWM signals in order to generate an effectively higher DPWM resolution. Thus, in this method, the duty cycle is varied between two switching periods so that the average duty cycle has a value between two adjacent quantized duty cycle levels as shown in Figure 2.9. Let D_o and D_{o1} correspond to two quantized duty cycle levels from the DPWM module such that, $D_{o1} = D_o + \text{LSB}$. If D_o is put out in three subsequent switching periods, followed by one period of D_{o1}, then the average value of the duty cycle will be $D_{average} = D_o + \frac{1}{4}\text{LSB}$. The averaging action is implemented by the output filter. If the DPWM is made to alternate between D_o and D_{o1} every next switching period, then the average duty cycle is $D_{average} = D_o + \frac{1}{2}\text{LSB}$. It has been shown that by using dither pattern spanning 2^M switching periods, the effective DPWM resolution can be improved by M bits.

$$n_{dpwmeff} = n_{dpwm} + M \quad (2.9)$$

However, the disadvantages of dithering method are low bandwidth and low frequency ripple.

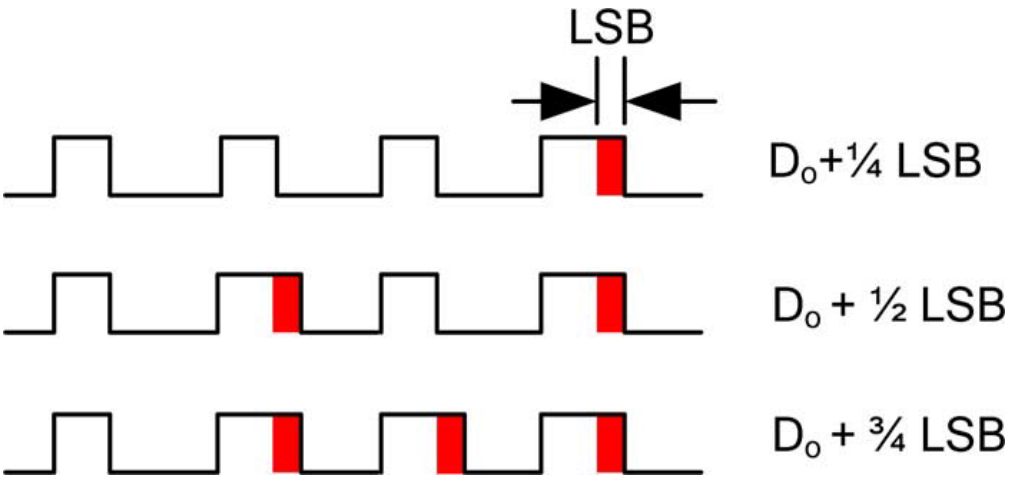

Figure 2.9: Scheme of digital dithering [3]

2.3.2.2 Sigma Delta Modulation

It has been demonstrated in [14-16] that high performance DC-DC conversion, which depends on a high resolution DPWM, can be achieved by a very simple, low resolution DPWM with multi bit digital sigma delta preprocessing. In this method, the DPWM duty cycle command is pre-processed by a multi bit digital sigma delta modulator, as shown in Figure 2.10, so that the DPWM quantization noise will be shaped in frequency. As a result, the total quantization noise at the output of the DC-DC converter is reduced, and the effective resolution of the DPWM in the control loop is increased dramatically.

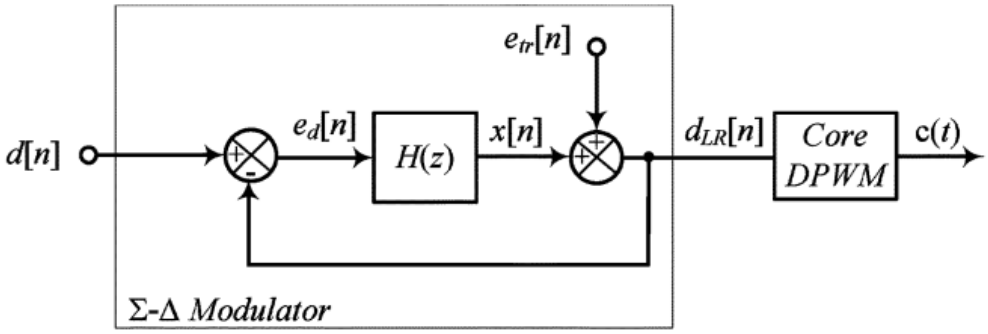

Figure 2.10: Multi bit digital sigma delta modulator [16]

The z transform of $d_{LR}[n]$ becomes

$$D_{LR}(z) = \frac{H(z)}{1 + H(z)} D(z) + \frac{1}{1 + H(z)} E_{tr}(z) \tag{2.10}$$

This equation shows that $H(z)$ influences the truncated signal. When $H(z)$ is large in amplitude, the high resolution input is almost unchanged and the quantization error is suppressed. Consequently $d_{LR}[n]$ becomes approximately equal to the high resolution input $d[n]$. The part of the equation describing the error attenuation is given by

$$N_{TF}(z) = \frac{1}{1 + H(z)} \tag{2.11}$$

where $N_{TF}(z)$ is called the noise shaping transfer function whose order usually defines the order of the sigma delta modulator.

2.3.2.3 Other Schemes

Three different digital duty cycle modulation schemes are presented that improves the resolution in [17]. The three schemes are constant on time modulation, constant off time modulation and a combination of constant frequency and constant on time modulation. Ten times improvement in resolution is achieved by these schemes compared to constant frequency modulation. The paper [18] investigates the application of a mixed signal synchronous / asynchronous digital controller to DC–DC boost converters. The digital control synchronously generates current and voltage ramps by using two low resolution digital to analog converters. The turn on and turn off time of the switch are determined asynchronously by comparing the converter state variables and the digitally generated current and voltage ramps. The control features high dynamic performance, frequency modulation during transients, small quantization effects, and low complexity.

The design and implementation of a digitally controlled DC-DC converter that provides dynamically adjustable supply voltage for a radio frequency power amplifier is presented in [19]. In this application, the DC-DC converter has to

operate over a wide range of output voltages, and over a correspondingly wide range of output power. In this work a combination of constant frequency continuous conduction mode and a variable frequency discontinuous conduction mode is used to achieve very high converter efficiency over a wide range of output power levels. The variable frequency converter control is accomplished using a current estimator circuit, which eliminates the need for current sensing.

In general, all the techniques and their combinations reviewed above may be used in the application of digitally controlled DC-DC converter. Fast counter-comparator scheme is easy to use and simple to implement. Since it is fully digital logic circuits, it is very suitable for implementation in microprocessors, DSPs or FPGAs. However, when high resolution and high switching frequency is a must, extremely high clock frequency and power consumption will be disadvantageous. Both tapped delay line and ring oscillator MUX are implemented by analog method, so it is only suitable for mixed mode analog and digital implementation. The ring oscillator MUX scheme is well suitable for these applications with a multi-phase structure because of its symmetric structure. Soft methods like dithering and sigma delta modulation also can be utilized with the above mentioned hardware architecture to improve the resolution of DPWM and to save digital core area of the chip. As the demand for the implementation of high frequency digitally controlled DC-DC converter increases, research in fine resolution DPWM strategies will continue to be topics of great relevance. The uniqueness of this study is to improve the resolution of DPWM by soft method with significant reduction in conducted emissions.

2.4. Digital control algorithm

Substantial research work has been reported on advanced control algorithms that improve the performance of digitally controlled DC- DC converters. Basically, they fall into two classes: linear control method and non-linear control method. Linear digital control methods are translated directly from the techniques, which are widely used in analog control circuits, and provide comparable performance. To achieve faster transient response, other non-linear control techniques, such as

predictive control, sliding mode control, adaptive control and hysteretic control have been implemented. This section will briefly review these aspects.

2.4.1 Proportional integral derivative controller

The dominant approach to the modeling and controller design of switched mode DC–DC converters is the method of state space averaging and the design of a control loop comprises of a Proportional Integral Derivative (PID) type controller and a PWM unit. Two main strategies have been used in order to design the output voltage control loop, namely, analog to digital redesign or direct digital design. In the first case the control loop is first designed in the s-domain using traditional techniques, and subsequently a digital controller is obtained using some of the s-domain to z-domain transformation methods. In the direct digital design, the discrete controller is directly designed in the z-plane by using a discrete small signal model of the converter.

In [20], an exact small signal discrete time model is proposed for digitally controlled DC-DC converter. The model, which is based on discrete time modeling and the standard *Z* transform, takes into account the modulator effects and the delays in the control loop. A direct digital design method is used to derive the transfer function in the *z*-domain, which can be formatted to a difference equation for implementation. A PID controller calculates a new value of duty cycle, $\mathrm{dc}[\mathrm{n}]$, that controls the DPWM, according to

$$\mathrm{dc}[\mathrm{n}] = \mathrm{dc}[\mathrm{n}-1] + \mathrm{ae}[\mathrm{n}] + \mathrm{be}[\mathrm{n}-1] + \mathrm{ce}[\mathrm{n}-2] \qquad (2.12)$$

where $\mathrm{e}[\mathrm{n}], \mathrm{e}[\mathrm{n}-1], \mathrm{e}[\mathrm{n}-2]$ are the consecutive samples of the error signal. In [21] a new exact small signal domain model is derived that gives rise to the development of a uniformly sampled PWM equivalent of the converter. In [22] a time domain design method for the digital controller of PWM DC–DC converters was developed. In [23], based on the above reported work, a digital controller is implemented for multiple output buck converter using 16-bit microcontroller. A modular design of embedded feedback controllers using Field Programmable Gate Array (FPGA) technology is studied in [24]. In this work, a novel distributed arithmetic based PID controller algorithm is proposed and integrated into a digital

feedback control system that has demonstrated 80% savings in hardware utilization and 40% savings in power consumption compared to the multiplier based scheme. The complete design and implementation of a digital controller for a high frequency switching power supply is given in [25]. The controller design is based on direct digital design approach and standard root locus techniques. Guidelines for the minimum required resolution of fixed point computational unit are also derived. A similar approach is followed in this thesis for the design of the compensator. The correlation between the discrete coefficients of (2.12) in discrete-time and the equivalent continuous-time compensation has been done using the pole-zero matching technique [19]. Analyzing the digital PID compensator using an equivalent continuous time model equation (2.12) can be rewritten as

$$dc[n] = dc[n-1] + K\left(e[n] - 2r\cos\left(2\pi\frac{f_z}{f_{sw}}\right)e[n-1] + r^2 e[n-2]\right) \tag{2.13}$$

where

$$r = \exp\left(\frac{-\pi f_z}{Q_z f_{sw}}\right) \tag{2.14}$$

Q_z and f_z are the characteristic of the zeros. f_{sw} is the switching frequency.

With advances in digital control for high frequency switched mode converters, new possibilities arise to consider practical realizations of more advanced control approaches. The advanced control algorithm so far carried out in the area of digitally controlled DC-DC converter is presented in the subsequent section.

2.4.2 Improved transient response

For a DC-DC converter there exists a best possible dynamic response/optimality condition to a load current transient of any magnitude. Under this optimality condition, the shortest recovery time and the smallest overshoot/undershoot during the transient are achieved simultaneously. A digital control algorithm capable of separately specifying the desired output voltage and transient response for a synchronous buck converter operating in voltage mode was

developed in [26]. In this work, the duty cycle is controlled by comparing an artificial saw tooth wave against a reference voltage, V_{ref}. In this work an algorithm is used that superimposes a small control signal onto the voltage reference at each switching cycle to cancel out the perturbations. For the nominal reference voltage, V_{ref}, the nominal duty cycle is given by

$$D = \frac{V_{ref}}{V_p} \tag{2.15}$$

where V_p is the amplitude of the sawtooth waveform. The control variable, v_{ref}, is composed of the steady state term V_{ref} and a perturbation $\hat{v}_{ref}$. Every switching cycle, the ADC samples the inductor current and the output voltage and computes the value of v_{ref}. By this method the desired output voltage and the type of transient response that the regulator would exhibit can be precisely specified. A zero steady state error in the output voltage can be obtained with the aid of additional dynamics to allow the controller to track a load change and update the reference to a new load state. The specifications of the control algorithm are achieved by pole placement using complete state feedback.

It is demonstrated in [28], [29], that by implementing two separate control strategies for steady state and transient conditions, the overall dynamic performance of the converter can be improved. In [28], two separate sets of linear PID compensators are implemented digitally to provide larger bandwidth during transient conditions. While transient response is improved in [28], the controller is still subject to the limitations of slow compensator networks. In [29], a method combining linear voltage mode control and non-linear hysteretic control is introduced. While this method does improve dynamic response, the controller tends to "over compensate" for load current variations, causing the output voltage to over shoot after it recovers from a voltage drop, thereby resulting in large settling times.

In [30], a new optimal control algorithm to improve the dynamic performance of DC-DC converters is proposed. Using the principle of capacitor charge balance, the minimum number of switching cycles and their respective duty cycles are predicted in order to minimize the output voltage overshoot/undershoot and to drive the output voltage back to its nominal value in the shortest possible

time during load transient conditions. By utilizing the proposed algorithm, the output capacitor size can be significantly reduced while still meeting the voltage tolerance requirements.

In [31], a voltage mode digital controller for low power high frequency Switched Mode Power Supplies (SMPS) that has fast transient response, approaching physical limitations of a given power stage, is proposed. In steady state, the controller operates as a conventional pulse width modulation regulator and during transients it utilizes a novel fast voltage recovery mechanism, based on real time processing of the output voltage in digital domain. This continuous time digital signal processing mechanism is implemented with a very simple processor consisting of a set of asynchronous comparators, delay cells, and combinatorial logic. To eliminate the need for current measurement and calculate the optimal switching sequence of the power stage transistors, the processor performs a capacitor charge balance algorithm, which is based on the detection of the output voltage peak/valley point. An approach to near time optimal control for synchronous buck DC–DC converters is proposed in [32]. In this work the proposed proximate time optimal digital controller is a combination of a linear PID compensator close to a reference point, and a linear or nonlinear switching surface controller away from the reference, together with smooth transitions between the two. A hybrid capacitor current estimator enables switching surface evaluation and eliminates the need for current sensing. A similar hybrid digital adaptive control for fast step load transient responses in synchronous buck DC-DC converters is presented in [33]. The proposed controller results in near time optimal step load transient responses even when the output voltage is sampled using a relatively low resolution, narrow range window ADC. The controller is a combination of a standard constant frequency PWM control in the vicinity of steady state operating point and a bank of switching surface controllers away from the reference. Here, the switching surface slope is adaptively selected by a supervisor based on an inductor current estimate. Furthermore, the controller is capable of taking into account a maximum inductor current limitation. In those applications where a high current slew rate at low output voltage is required, a combined linear-non-linear control is proposed in [34]. This significantly reduces the output recovery time in

comparison with a conventional linear control. In [35] the stability of the linear-non-linear control under fixed load condition and under four load current steps are presented. A nonlinear digital control of a boost converter based on a sliding discrete-time approximation to achieve fast response is presented in [36]. This controller is based on an inner nonlinear current control loop and an outer discrete PI voltage control loop. The inner loop is designed following a discrete time sliding mode concept.

In order to overcome the bandwidth limitation caused by additional phase delay, an adaptive third order digital controller has been introduced in [37]. However, in this method, both ADC and digital controller should be clocked at double the switching frequency.

The inherently nonlinear characteristics of DC–DC converters have also drawn greater attention. In particular, research has been directed at applying non-linear control principles to the regulation and dynamic control of converter output voltage. It is known that non-linear control is capable of improving the dynamic response of a converter since it is able to quickly react to transient conditions. A general purpose controller for DC–DC converters based on the fuzzy logic is presented in [38]. As compared to standard controllers, it provides improved performances in terms of overshoot limitation and sensitivity to parameter variations. This is possible since fuzzy logic control rules can be assigned separately for the various regions of operation, resulting in effective small signal and large signal operation. In [39] the implementation of a fuzzy controller for DC-DC converter using an inexpensive 8-bit microcontroller is presented. In [40], digital controller is presented that behave as a linear controller for conditions when the output voltage error is small and a non-linear controller when the output voltage error is large. This is accomplished in [40] by use of a PI like fuzzy logic controller and non-uniform fuzzy sets. The controller mimics a PI controller during steady state conditions; however, when either the output voltage error or derivative of the output voltage is relatively high, the duty cycle varies at a faster non-linear rate.

2.4.3 System identification/Integration of frequency response measurements

System identification is the most attractive control methods of digitally controlled DC- DC converter. In these methods system parameters are extracted from information available in feedback loop and, accordingly, the control law is adjusted to improve the system robustness, dynamic response, and regulation. In general, system identification is divided into parametric and non-parametric methods. In parametric methods, a system model is assumed, and the identification amounts to an estimation of the model parameters. In non-parametric methods, no assumption is made about the system model, and the identification is used to directly compute the system frequency responses. Nonparametric methods include: correlation analysis, transient-response analysis, and frequency response (Fourier or spectrum analysis). In [41], a modified cross correlation approach for system identification together with experimental results from an FPGA based digital controller realization is presented. Modified cross correlation is achieved by first injecting multi period pseudo random binary signals (PRBS), meaning that a single period PRBS is repeated identically a finite number of times, then averaging the cross correlation of the input and the output over several PRBS periods. This approach rejects noise sources and results in accurate system identification. During the perturbation process, to obtain accurate information, the system should operate in steady state. As a result, these approaches are best suited for one-time frequency response measurement. The hardware is still fairly complex for the use in very low power applications.

Let $\mathrm{y(n)}$ be the sampled output signal, $\mathrm{u(k)}$be the input digital control signal, $\mathrm{h(k)}$ be the discrete time system impulse response, $v(\mathrm{n})$ be the noise, then

$$y(\mathrm{m}) = \sum_{\mathrm{k}=1}^{\infty} \mathrm{h}(k)\mathrm{u}(\mathrm{n}-\mathrm{k}) + \mathrm{v}(\mathrm{n}) \tag{2.16}$$

If the input control signal is considered to be white noise, then the cross-correlation between the input and output sampled signals, give the discrete time

system impulse response. The cross correlation of the input control signal u(k)and the output y(n) is given by

$$R_{uy}(m) = \sum_{n=1}^{\infty} u(n)y(n+m) \tag{2.17}$$

$$R_{uy}(m) = \sum_{n=1}^{\infty} h(n)R_{uu}(m-n) + R_{uv}(m) \tag{2.18}$$

where $R_{uu}(m)$ is the auto-correlation of the input signal. If the input signal is selected to be white noise, then

$$R_{uu}(m) = \delta(m)\ ,\ R_{uv}(m) = 0 \tag{2.19}$$

Under this condition, equation (2.24) reduces to

$$R_{uy}(m) = h(m) \tag{2.20}$$

In [42] [73], the feasibility of incorporating fully automated frequency response measurement capabilities in digital controllers for PWM DC–DC converters at low additional cost has been done. This work presents a practical, hardware efficient implementation of correlation based system identification for PWM DC-DC power converters, adapting methods from the audio engineering field to reduce the effects of ADC quantization to obtain an accurate and smooth system frequency response. The approach is completely automated online and can be applied to a wide range of PWM DC–DC converter architectures with no changes to the identification algorithm. An FPGA based digital network analyzer for digitally controlled SMPS, has been implemented in [43]. Similar to standard network analyzers, the digital network analyzer can be used to validate converter models and the system design. The digital network analyzer can be built into the digital controller, resulting in an accurate measurement of the actual delays and non-idealities in the sampling and digital hardware.

2.4.4 Auto tuning

Approaches to monitoring and/or tuning of controller parameters in response to the actual system dynamics is presented in [44]- [50],[77].

2.4.4.1 Auto tuning based on relay feedback

In [44],[77] the relay feedback based tuning technique identifies the key , properties of the process by inducing amplitude controlled limit cycle oscillations and measuring the corresponding oscillating frequencies. The tuning operates in closed loop configuration with a relay block inserted in the feedback loop. A relay is an instantaneous non-linear system implementing the function, $e_r = f_r(e)$, defined as

$$e_r = f_r(e) = \begin{cases} +A_r, & e > 0 \\ -A_r, & e \leq 0 \end{cases} \tag{2.21}$$

with $A_r > 0$ defined as the relay amplitude. When inserted into an existing feedback loop the strong non-linearity of the relay triggers a limit cycle oscillation whose frequency and amplitude carry information related to the plant which can be used in tuning purposes. The frequency at which such limit cycle oscillation, f_{osc}, sustains itself fulfill the requirements that

$$< G_c(f_{osc}) + < T_u(f_{osc}) + < F(f_{osc}) = -\pi \tag{2.22}$$

where $G_c(z)$ represents the compensator transfer function, $T_u(z)$ represents the uncompensated small signal transfer function of the converter and $F(z)$ is the transfer function of the filter superimposed between the compensator and the power converter.

In the case of relay, using the describing function method the amplitude balance equation is given by

$$\frac{4A_r}{\pi a_{osc}} T_{ufosc} F_{fosc} = 1 \tag{2.23}$$

where a_{osc} represents the amplitude of oscillation at the error signal, T_{ufosc} and F_{fosc} are amplitude of $F(z)$ and $T_u(z)$ at f_{osc}. In this work the compensator is implemented in the programmable cascade form

$$G_c(z) = \frac{K_i}{1 - z^{-1}} (1 - k_1 + k_1 z^{-1})(1 - k_2 + k_2 z^{-1}) \tag{2.24}$$

The tuning approach is a three step procedure. The first zero of the compensator is placed at the resonant frequency of the converter LC filter. The limit oscillation frequency, f_{osc}, is very close to the resonant frequency and can be used to identify the converter resonant frequency. The oscillator frequency, f_{osc}.is measured digitally. Then the value of k_1 is computed as given below.

$$k_1 = -\frac{1}{2\pi}\frac{f_{sw}}{f_{osc}} \tag{2.25}$$

where f_{sw} is the switching frequency. The PID integral gain K_i is tuned for the desired cross over frequency. The amplitude of the oscillation, a_{osc}, is measured and K_i is tuned as per the equation given below

$$K_i \leftarrow \frac{4A_r F_{fosc}}{\pi a_{osc}} K_i \tag{2.26}$$

2.4.4.2 Injection based auto tuning

A practical injection based method for continuous monitoring of the crossover frequency and phase margin is proposed in [45]. The proposed approach is derived from Middlebrook's loop gain measurement technique [46], adapted to a digital controller implementation. A digital square wave signal,$u_{pert}[k]$, is injected into the feedback loop, superimposed to the PID output, $u_y[k]$. The overall control command that modulates the converter is therefore

$$u_x[k] = u_y[k] + u_{pert}[k] \tag{2.27}$$

Simultaneously, signal $u_y[k]$ and $u_x[k]$ before and after the injection point is measured. The system loop gain is found by evaluating the magnitude and phase relationship between $u_y[k]$ and $u_x[k]$ at the injection signal frequency. The compensator gain is adjusted until the correct amplitude and phase relationships are established between the AC components of $u_y[k]$ and $u_x[k]$. The required is adjusted while monitoring loop signals to obtain the system crossover frequency and phase margin online, i.e., during normal closed loop SMPS operation. If the system loop gain is $T(z)$, the tuning target can be expressed as

$$T\left(e^{j\omega_c T_s}\right) = -e^{j\varphi_m} \tag{2.28}$$

where ω_c is the predefined bandwidth and φ_m is the phase margin. The proposed approach does not require open loop or steady-state SMPS operation and is capable of convergence in the presence of load transients or other disturbances.

In [47], a closed-loop self-tuning technique for digitally controlled DC-DC switched mode power supplies (SMPS) based on PID regulators, which derives from the more general model reference auto tuning techniques is presented. After briefly discussing an open loop, model reference based tuning technique, a closed loop solution is presented in which a perturbation frequency generated digitally is injected into the control loop and superimposed to the duty cycle command. The tuning is performed elaborating the signals right before and right after the injection point, and adjusting the PID parameters until predefined bandwidth and phase margin targets are obtained. The proposed approach allows for a robust and repeatable tuning, mainly because of the high resolution and dynamics available at the signal injection point. Moreover, the tuning is performed maintaining the closed loop configuration, thus ensuring voltage regulation even during the PID adjustment, this being a fundamental constraint for most electronic equipment.

2.4.4.3 Programmable PID structure

A hardware description language coded auto tuning algorithm for digital PID controlled DC–DC power converters based on online frequency response measurement is presented in [48] [73]. The algorithm determines the PID controller parameters required to maximize the closed loop bandwidth of the feedback control system while maintaining user specified stability margins and integral based no limit cycling criteria, as well as ensuring single crossover frequency operation and sufficiently high loop gain magnitude at low frequencies.

Online adaptive tuning technique for digitally controlled SMPS have been presented in [49]. The approach is based on continuous monitoring of the system crossover frequency and phase margin, followed by a Multi Input–Multi Output (MIMO) control loop that continuously and concurrently tunes the compensator parameters to meet crossover frequency and phase margin targets. Continuous

stability margin monitoring is achieved by injecting a small digital square wave signal between the digital compensator and the DPWM. The MIMO loop adaptively adjusts the compensator parameters to minimize the error between the desired and measured crossover frequency and phase margin**.** An approach to adaptive tuning of voltage mode digital controllers for SMPS in the presence of large signal changes from discontinuous conduction mode (DCM) to continuous conduction mode (CCM) and vice versa is presented in [50]. The approach is capable of maintaining a high performance control loop without the stability issues related to DCM to CCM mode transitions. The adaptive tuner, modeled as a MIMO controller, is designed to continuously adjust the parameters of a PID compensator such that crossover frequency and phase margin measured by the digital controller match desired values. A simplified design procedure for the adaptive tuning system is proposed that reduces the small signal MIMO design into two independent single input, single output control loops.

2.5 Reduction in conducted emission by the modulation of switching frequency

In this work, reduction in conducted EMI is also aimed at. Hence this section gives the EMI mitigation techniques so far implemented in the area of digitally controlled DC-DC converter.

Switching power converters have been reported to generate common mode and differential mode conducted noise in addition to radiated noise. DC-DC power converters are powerful sources of electromagnetic interferences because of the large di/dt and dv/dt. As a result, EMI becomes an inevitable concern in the design of high frequency converters. The classical way of EMI suppression is accomplished by the isolation of noise coupling path, suppression of noise source, filters and shielding.

Alternative, EMI mitigation techniques that eliminate the need for EMI filters by spreading the switching converters noise over a frequency range has been extensively investigated in [51] – [58]. By using these techniques, the noise generated by the SMPS can be spread across a frequency band. As a result, the

average spectral power density of the broadband noise can thus be drastically reduced. Thus the conducted emissions of a switching power circuit can be reduced by the modulation of the PWM switching frequency. The modulating parameters must be properly chosen to have effective EM1 reduction without causing significant side effects, such as audible noise due to frequency variation and poor converter output voltage regulation. Frequency modulation (FM) and random switching methods have been used for reducing conducted EMI in power converters. The effectiveness of frequency modulation in reducing the fundamental harmonic is presented in [51]. By modulating the switching frequency, side bands are created and the emission spectrum is broadened. The power is distributed around many side band frequencies. The general analytical expression for frequency modulation or phase modulation is given by

$$F(t) = A_c \cos\left[2\pi f_c t + \frac{\Delta f}{f_m}\sin(2\pi f_m t)\right] \tag{2.29}$$

where A_c and f is the amplitude and frequency of the carrier signal, f_m is the frequency of the modulating signal. Let β ($\beta = \frac{\Delta f}{f_m}$) be the modulation index, then the energy of the fundamental component is spread into a band B given by

$$B = 2f_m(1 + \beta) \tag{2.30}$$

Frequency modulation using three periodic patterns- sinusoidal, exponential and triangular, for the modulating function are presented in [52]. In the buck converter an EMI reduction of 10 dB approximately has been obtained in the full frequency range of conducted EMI for all the three periodic patterns. But, the best performance is given by the triangular profile and the worst, by the exponential profile. This in accordance with the attenuation theoretically computed. In [53], the theoretical power spectrum for standard constant frequency pulse width modulation scheme and the FM scheme has been derived.

For a typical PWM signal, G(t), with duty cycle D and switching period T_s, G(t) may be mathematically expressed by Fourier series [53]

$$G(t) = \sum_{n=-\infty}^{\infty} C_n e^{j\theta_n} \tag{2.31}$$

where C_n and θ_n are the magnitude and phase of the n^{th} harmonic. C_n is given by

$$C_n = \frac{1}{T_s}\int_{-T_s/2}^{+T_s/2} G(t)e^{-j2\pi nft}\,dt \tag{2.32}$$

For periodic frequency modulation of switching frequency, $G(t)$ can be given by

$$G(t) = \sum_{n=-\infty}^{\infty} C_n e^{jn2\pi f_{sw}t}\{\cos\lceil n\beta \sin(2\pi f_m t)\rceil + j\sin\lceil n\beta \sin(2\pi f_m t)\rceil\} \tag{2.33}$$

By using Jacobi equation, the cosine and sine terms can be expressed as

$$\cos\lceil n\beta \sin(2\pi f_m t)\rceil = J_o(n\beta) + \sum_{k=even}^{\infty} 2J_k(n\beta)\cos(2\pi k f_m t) \tag{2.34}$$

$$\sin\lceil n\beta \sin(2\pi f_m t)\rceil = \sum_{k=0dd}^{\infty} 2J_k(n\beta)\sin(2\pi k f_m t) \tag{2.35}$$

where $J_k(.)$ is the k^{th} order Bessel function given by

$$J_k(n\beta) = \left(\frac{n\beta}{2}\right)^k \left[\frac{1}{k!} - \frac{(n\beta)^2}{1!\,(k+1)!} + \frac{(n\beta)^4}{2!\,(k+2)!} - \cdots\right] \tag{2.36}$$

The magnitude of $G(t)$ at frequency f, $G(f,\beta)$, can be shown to be

$$G(f,\beta) = \sum_{n=-\infty}^{\infty} C_n\{J_o(n\beta)\delta(f - nf_{sw}) + \sum_{k=1}^{\infty} J_k(n\beta)\delta(f - nf_s - kf_m) + (-1)^k \delta(f - nf_{sw} + kf_m)\} \tag{2.37}$$

The power spectrum $S_G(f,\beta)$ in the positive range is given by

$$S_G(f,\beta) = 2\left|\sum_{n=1}^{\infty} C_n\{J_o(n\beta)[\delta(f - nf_{sw}) + \sum_{k=1}^{\infty} J_k(n\beta)\delta(f - nf_{sw} - kf_m) + (-1)^k\delta(f - nf_{sw} + kf_m)]\}\right|^2, f > 0 \tag{2.38}$$

Thus $S_G(f,\beta)$ contains infinite discrete harmonics and is dependent on β and f_m.

For the standard PWM scheme, $\beta = 0$ and only $J_0(0)$ exists. Then $S_G(f,\beta)$ becomes

$$S_G(f,\beta) = 2\sum_{n=1}^{\infty}|C_n|^2\delta(f - nf_{sw}) \tag{2.39}$$

In [53], the spectral characteristics of Random Carrier Frequency modulation (RCFM) is also presented. The analysis provides a theoretical platform for studying the characteristics of this random switching scheme. The RCFM scheme has been compared with the standard constant frequency pulse width modulation scheme and the FM scheme. Comparisons of their spectral performance show that the RCFM scheme has better conducted EMI suppression than the FM and standard PWM schemes.

For the RCFM, switching period T_s is dithered in random manner and the duty ratio D is kept constant. Instead of using power spectrum, PSD is

$$S_G(f,\Re) = \frac{1}{E[T_k]}\left\{E[|G(f)|]^2 + 2\,\mathrm{Re}\left\{\frac{E\left[G(f)e^{j2\pi fT_k}\right]E[G^*(f)]}{1 - E[e^{j2\pi fT_k}]}\right\}\right\} \tag{2.40}$$

where $G^*(f)$ is the complex conjugate of $G(f)$ and T_k is the instantaneous switching period. The probability density function of T_k, $P(T_k)$, is of uniform distribution with the expected value of T_s, $E(T_s)$.

It is defined as

$$P(T_k) = \frac{1}{\Re E(T_s)} \tag{2.41}$$

where $\Re$ is the level of random ness.

In [54], also, a detailed analysis and the spectral characteristics of a Random Carrier Frequency (RCF) technique for suppressing conducted EMI in an offline SMPS is presented. The effect of the level of randomness on the degree of spectrum spreading are also studied.

A spread spectrum technique and system for reducing average EMI in low power digitally controlled DC-DC SMPS are introduced in [55]. The technique utilizes very simple hardware, where the switching frequency of a SMPS is dynamically varied over a controlled range. This is achieved by changing the supply voltage of a ring oscillator based digital pulse-width modulator in a pseudo random

fashion, through 128 discrete steps. A reduction of 23 dB in the conducted EMI with an efficiency degradation of less than 0.1% was obtained, compared to fixed frequency operation.

Meanwhile, an analysis and experimental results of the Random Pulse Width Modulation (RPWM) and Random Pulse Position Modulation (RPPM) methods for DC–DC converters have been presented in [56]. In this the characteristics and performance of power converters under two randomized modulations are evaluated. The theoretical relationships of discrete harmonics, continuous noise and output voltage ripple of the RPWM and RPPM schemes are established and compared with those of a standard deterministic PWM scheme in a buck converter. The performance of the RPPM method is found to be closer to the standard PWM method than that of the RPWM method. For DC–DC power conversion, the RPPM method offers much better output voltage performance than the RPWM method.

An evaluation of the spectral characteristics of switching converters with a Chaotic Carrier Frequency Modulation Scheme (CCFMS) has also been reported in [57]. The property of frequency spreading in CCFMS is studied by using statistical analysis method. The CCFMS is found to exhibit similar behaviors as the RCFM in the high frequency range, but CCFMS introduces lower level of low frequency harmonics at the output than that of the RCFM.

The effects of the switching frequency modulation on the output voltage was studied and reported in [58]. The output voltage ripple for continuous mode can be ideally calculated as follows:

$$\frac{\Delta v_o}{v_o} = \frac{\pi^2}{2}\,(1 - D)\left(\frac{f_{LC}}{f_{sw}}\right)^2 \qquad (2.42)$$

where $f_{LC} = \frac{1}{2\pi\sqrt{LC}}$ is the corner frequency of the output low-pass filter consisting of an inductor L and a capacitor C, and f_{sw} is the switching frequency. Since v_o, D, and f_{LC} are constant parameters, output voltage ripple Δv_o only depends on f_{sw}. If f_{sw} is constant (as in the non-modulation case), output voltage ripple remains constant; however, if $f_{sw}$is frequency modulated, then Δv_o oscillates as a function

of f_{sw}. Direct transformation of fixed frequency into modulated frequency designs must be carefully analyzed, mainly if output voltage ripple is a restrain.

A novel control technique called Bi-Frequency Pulse Train (BF-PT) control is proposed in [59] to improve light-load efficiency and EMI emission. In BF-PT control, the output voltage of switching DC-DC converter is sampled at the beginning of each switching cycle and compared with a reference voltage to determine whether a high or low frequency control pulse should be selected as the control pulse. The BF-PT control realizes output voltage regulation by employing high and low frequency control pulses instead of adjusting the duty ratio of the control pulse cycle by cycle. In this work, the two types of control pulses with different switching frequencies spread the emission spectrum over discrete frequencies resulting in lower EMI. Low frequency control pulses at lighter load improve the light load power conversion efficiency. A similar Peak Current Mode Bi-Frequency control (PCM-BF) for switching DC-DC converters operating in the discontinuous conduction mode is proposed in [60]. In the PCM-BF control scheme there are two control loop, the voltage and current loop. The voltage loop is used to determine whether high or low frequency control pulse should be generated as control pulse, and the current loop is used to determine the ON time of the control pulse during the switching cycle. A practical optimization of EMI reduction is also done in [61] by mathematically modelling the EMI receiver rather than the theoretical power spectrum density and then optimizing the EMI for a well-defined value of the modulation index. A reconfigurable periodic Bi-Frequency DPWM (BF-DPWM) with custom harmonic reduction is presented in [62]. The proposed BF-DPWM would achieve considerable harmonic reduction and improved DPWM resolution with an insignificant ripple impact.

The use of digital controllers in DC-DC converters will become essential not only to meet the core powering requirements but also to significantly improve system diagnostics with system level power management. These digital control systems present few disadvantages in comparison with analog ones. The finite word length of digital controller, limit cycle oscillation due to the quantization of the ADCs & DPWMs and the computational delays in the control loop are some of the

disadvantages. The research works [1-49] aims at the optimization of the design of high frequency ADC, high frequency DPWM and control law. Whereas the present work deals with the realization of a high frequency digitally controlled DC-DC converter that requires low resolution ADC and DPWM without sacrificing the performance of the converter.

CHAPTER 3

Reduction of limit cycle oscillation due to low resolution ADC using reduced state Kalman filter

This chapter presents a method to reduce the limit cycle caused by low resolution ADC in digitally controlled DC-DC converter. In this chapter a reduced state Kalman filter is proposed to get the optimum estimate of the output voltage from the noisy measurement provided by the low resolution ADC. The reduced state Kalman filter, with offline computation of the coefficients reduces the computational complexity of the Kalman filter and makes it suitable for the real time application of estimating the output voltage from a noisy measurement. The contributions of the research work are summarized as follows:

i. The reduced state Kalman filter is proposed to reduce the limit cycle oscillations caused by low resolution ADCs in digitally controlled DC-DC Converter.
ii. The reduction in state of the converter has facilitated the minimization of the clock cycle required for computation. This has been achieved by reducing the vector states of converter to scalar state and by computing the Kalman gain offline.
iii. The reduced state Kalman filter is simulated with 6-bit ADC in MATLAB environment and validated with different resolutions (5-bit, 6-bit, 7-bit and 8-bit) using prototype model, which is implemented using 16 bit DSP processor. The results show that the proposed scheme reduces limit cycle oscillation significantly and is computationally very efficient.

An ideal quantizer can be considered as a linear system with unity gain. As explained in Chapter 2, the quantization effect has been investigated using describing function approach in [4]. As explained in Appendix 1, the method represents the effective gain as a function of the amplitude of sinusoidal input signal

and DC offset bias. The amplitude and offset dependent gain of a quantizer can be significantly greater than unity as the offset approaches q/2, where q is the quantization level ($q = \frac{V_m}{2^{n_{adc}}}$, v_m is the full voltage range of the ADC and n_{adc} is the resolution of the ADC) [4]. For high resolution ADC, zero offset describing function is normally used. However, for low resolution ADC, the amplitude and offset dependent "gain" can be very high, which results in limit cycle oscillation even if the resolution of DPWM is high. This occurs in particular cases where the reference voltage of the converter is such that the output voltage does not result in zero error voltage due to the quantization effect of low resolution ADC. Similarly, the usage of high resolution ADC and low resolution DPWM can result in limit cycle oscillation [4]. However, no detailed studies are reported to express the elimination of limit cycle oscillation associated with low resolution ADC.

Meanwhile, the Kalman filters are effectively used to estimate the signal embedded in noise, where the signal is characterized by a dynamical or state model [63]. If the signal and noise are jointly Gaussian, then the Kalman filter is an optimal Minimum Mean Square Error (MMSE) estimator, and if not, it is the optimal linear MMSE estimator. Generally, the Kalman filter uses the dynamical model of the system and the measurements to form an optimal estimate of the state of the system. The Kalman filter model assumes that the state of the system to be estimated, can be represented by the state space model given by

$$x_k = Ax_{k-1} + Bu_k + w_k \tag{3.1}$$

x_k is the state vector, A is the state transition matrix, B is the control input matrix, u_k is the vector containing control inputs, w_k is the vector containing the process noise.

And that the measurements of the system can also be modelled as per the equation given by

$$y_k = Cx_k + v_k \tag{3.2}$$

where y_k is the vector of measurements, C is the transformation matrix that maps the state vector parameters into the measurement domain, v_k is the vector of

measurement noise. Then the Kalman filter will provide an optimum estimate of the state of the system, $\widehat{x_k}$, recursively over time by using the incoming measurement on y_k and the mathematical model process given by (3.1).

For high frequency switching converters, the implementation of Kalman filter to estimate the states of the converter is computationally complex and any delay would affect the phase margin of the converter. Thereby the performance of the converter will be affected. An optimal design of a Kalman filter has earlier been attempted with respect to its finite word length characteristics taking into account the round off noise due to state quantization [64]. But, no significant attempts were made to implement the Kalman filter with minimum clock cycle. Similarly, a state observer based sensor less control using Lyapunov method for boost converter is presented in [65]. The proposed controller was designed based on Lyapunov stability theorem which allows accurate output voltage tracking and stability by considering the large signal model and non-linearity of a boost converter operating only up to switching frequency of 50 kHz.

Thus a computationally efficient optimal implementation of Kalman filter for a high frequency digitally controlled DC-DC Converter is a major challenge. In this chapter a computationally efficient reduced state Kalman filter is proposed to reduce the limit cycle oscillations caused by low resolution ADCs in digitally controlled DC-DC Converter.

The chapter is organized as follows. In Section 3.1, the digitally controlled DC- DC converter using the proposed scheme is described. The modeling of the buck converter is given in Section 3.2. The reduced state Kalman filter used in the proposed scheme is presented in Section 3.3. In Section 3.4, simulation results are provided. In Section 3.5, the experimental results with detailed discussion are given. Section 3.6 presents the concluding remarks.

3.1 System description

Figure 3.1 shows the block diagram of a digitally controlled PWM DC-DC buck converter using the proposed scalar state scalar observation Kalman filter. In the feedback, the output voltage of the converter is scaled down, sampled and digitized using ADC which is a low resolution one. In general, the error is computed by taking the difference between the output of ADC and reference voltage (V_{ref}). Limit cycle oscillation may occur if the reference voltage is such that the quantized output voltage does not result in zero error voltage [4].

To avoid the limit cycle oscillation, the output of the ADC is fed to a reduced state Kalman filter, when the output is within a predefined limit (± 5 % of the rated value). The window for the output voltage is fixed based on the expected limit cycle amplitude at the output voltage. This ensures that the startup and dynamic performance of the converter are not affected by the introduction of the Kalman filter. The optimum estimate of the present value of output voltage is derived by adding the previous optimum estimate of the output voltage to the change in output voltage estimated by the reduced state Kalman filter. To get the optimum estimate of the change in output voltage, the difference between the present and previous sample of the output of ADC is given as the measured input to the Kalman filter and the small signal model of the converter is used to predict the change in the capacitor voltage. The Kalman filter gives the optimum estimate of the change in capacitor voltage, based on the predicted value given by the small signal model and the measured value. The optimal estimate of the change in capacitor voltage can be considered to be the same as that of the change in output voltage as the ESR of the output capacitor is low. The Kalman filter uses the weighted average method to give the optimal estimate of the change in capacitor voltage. The measurement on the change in output voltage will be noisy due to the low resolution of ADC. If the variance of measurement noise is more, the predicted value is given more weightage and vice versa. The estimated change in output voltage is added with the previous estimated value of the output voltage to get the present value of the output voltage.

The difference between this and the reference voltage is the error. The error thus computed is fed to a discrete time compensator. The discrete time compensator computes the digital duty cycle command based on one and two sample old duty commands, the present error, previous one and two samples old errors. This duty cycle command drives the digital pulse width modulator. A digital pulse width modulator outputs the gate drive pulses at the desired switching frequency based on the digital duty cycle command.

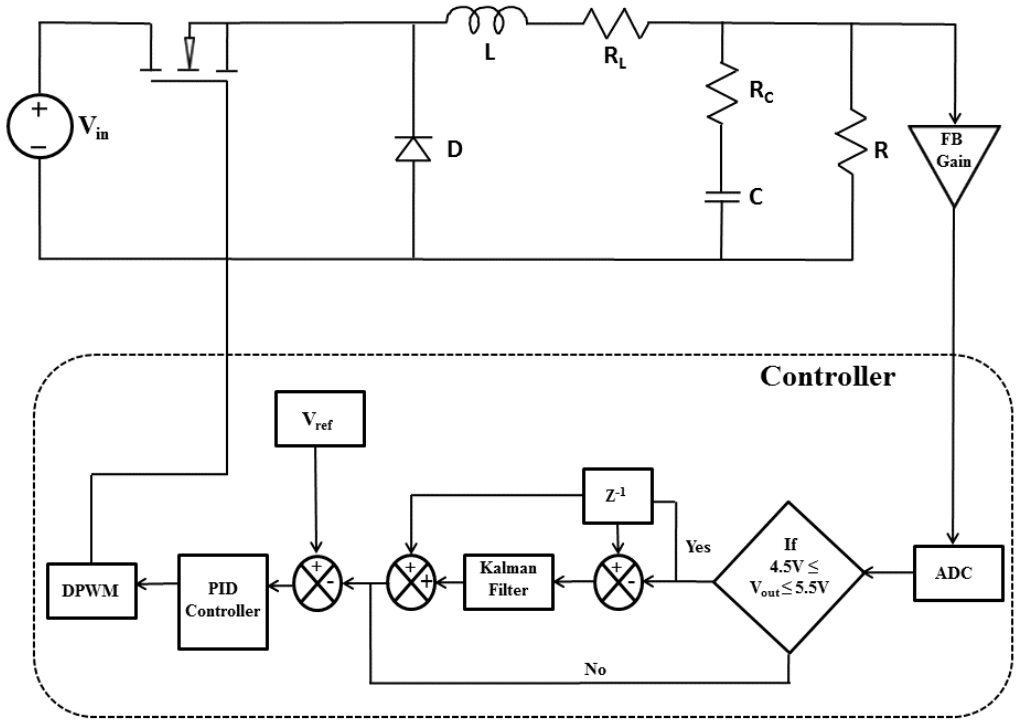

Figure 3.1: Block diagram representation of the proposed architecture

3.2 Modeling of buck converter

In this section, the small signal model of the DC-DC converter is quantitatively described. The two state variables, the change in inductor current ($\hat{i}_L(t)$) and capacitor voltage ($\hat{V}_c(t)$) are chosen. The state space model of the DC-DC converter is given by [20]:

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}\begin{bmatrix} \frac{d\hat{i}_L(t)}{dt} \\ \frac{d\hat{V}_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} (R_L + (R//R_C)) & -R/(R+R_C) \\ R/(R+R_C) & -1/(R+R_C) \end{bmatrix}\begin{bmatrix} \hat{i}_L(t) \\ \hat{V}_c(t) \end{bmatrix} + \begin{bmatrix} D \\ 0 \end{bmatrix}\hat{V}_{in}(t) + \begin{bmatrix} V_g \\ 0 \end{bmatrix}\hat{d} \quad (3.3)$$

where, $\hat{V}_{in}(t)$ is the change in input voltage, $\hat{d}$ is the change in duty cycle, D is the steady state Duty ratio, R_C is the Equivalent Series Resistance (ESR) of the output capacitor C, $R_L$is the series resistance of the output inductor L and R is the load resistance, $R//R_C$ is the equivalent parallel resistance of R and R_C.The change in output voltage derived from the small signal model is as follows:

$$\hat{V}_o(t) = (R//R_C)\hat{i}_L(t) + (R/(R+R_C))\,\hat{V}_c(t) \quad (3.4)$$

The equation (3.1) and (3.2) can be rewritten as

$$\begin{bmatrix} \frac{d\hat{i}_L(t)}{dt} \\ \frac{d\hat{V}_c(t)}{dt} \end{bmatrix} = [A]\begin{bmatrix} \hat{i}_L(t) \\ \hat{V}_c(t) \end{bmatrix} + [B]\begin{bmatrix} \hat{V}_{in}(t) \\ \hat{d} \end{bmatrix} \quad (3.5)$$

$$\hat{V}_o(t) = [C]\begin{bmatrix} \hat{i}_L(t) \\ \hat{V}_c(t) \end{bmatrix} \quad (3.6)$$

The equivalent discrete state equation of the converter model is obtained using zero order hold method.

$$A_d = e^{AT}\ ;\ B_d = \int_0^T e^{At}dtB\ ;\ C_d = C \quad (3.7)$$

The discrete time small signal model of the converter is derived using MATLAB. The general form of the discrete time small signal model of the converter is given by

$$\begin{bmatrix} i_L(n) \\ v_c(n) \end{bmatrix} = \begin{bmatrix} a_1 & a_2 \\ a_3 & a_4 \end{bmatrix}\begin{bmatrix} i_L(n-1) \\ v_c(n-1) \end{bmatrix} + \begin{bmatrix} a_5 \\ 0 \end{bmatrix}v_{in}(n-1) + \begin{bmatrix} a_6 \\ 0 \end{bmatrix}d(n-1) \quad (3.8)$$

In (3.8), the values of $a_i, (i = 1 \text{ to } 6)$ are functions of plant parameters. The variables $i_L(n)$ and $v_c(n)$ are the present value of the change in inductor current

and change in capacitor voltage respectively, $d(n-1)$and $v_{in}(n-1)$ are the previous value of the change in duty ratio and input voltage respectively.

The equivalent discrete time output equation of the converter can be written as

$$v_o(n) = cv_c(n) + c'i_L(n) \tag{3.9}$$

where, $c = R/(R + R_C)$ and $c' = R//R_C$

A necessary condition for the Kalman filter to work correctly is that the system for which the states are to be estimated, should be observable. The system is observable if and only if the observability matrix has rank equal to n where n is the order of the system (the number of state variables). The rank sufficiency of the Observability Grammian for the system represented by (3.8) and (3.9) justifies the use of Kalman filter for this application.

Equation (3.9) can be further modified by adding the measurement noise $v(n)$, which is given below:

$$v_o(n) = cv_c(n) + c'i_L(n) + v(n) \tag{3.10}$$

The measurement on the change in output voltage is noisy due to the quantization effect of ADC. The quantization noise of ADC can be considered as the measurement noise $v(n)$, and has uniform probability distribution between $-\frac{q1}{2}$ and $+\frac{q1}{2}$ where q_1 is the quantization level of the ADC. The quantization noise has zero mean and variance, ${\sigma_v}^2$, given by $\frac{{q_1}^2}{12}$.

3.3 Reduced state Kalman filter

In this section, to estimate the change in capacitor voltage $v_c(n)$, from the noisy measurement for the change in output voltage $\{v_o(0), v_o(1), \ldots v_o(n)\}$, the reduced state Kalman filter is proposed. The Kalman filter provides an optimal estimate of $v_c(n)$ of the converter by using the measurement of $v_o(n)$ and the prediction of $v_c(n)$ is given by the small signal model. The vector state has been reduced to the scalar state equation by considering only the change in capacitor

voltage $v_c(n)$. Based on (3.3), the prediction on the change in capacitor voltage using the small signal model requires the previous value of the change in inductor current and change in capacitor voltage.

In the proposed state reduction, the change in inductor current is modeled along with the process noise. The process noise $w(n)$ is introduced due to the quantizer, ADC and DPWM. The derivation of the process noise is dealt in Appendix 2. Therefore, the state equation of the change in capacitor voltage given in (3.3) can be considered to be a first order auto regression model and is given by

$$v_c(n) = a_4\, v_c(n-1) + w'(n) \tag{3.11}$$

where,

$$w'(n) = a_3 i_L(n-1) + w(n) \tag{3.12}$$

Based on (3.8), the noise contributed by $i_L(n-1)$ can be expressed as given below:

$$i_L(n-1) = a_1 i_L(n-2) + a_2 a_3 i_L(n-3) + a_2 a_3 a_4 i_L(n-2) + .. + a_5 v_g(n-1) + a_6 d(n-1) \tag{3.13}$$

Since $w'(n)$ is the sum of $w(n)$ and noise contributed by $i_L(n-1)$ which in turn is due to the sum of previous inductor current samples as given in equation (3.13), it is possible to assume that the noise in equation (3.12) is white Guassian noise, as per Central Limit theorem, with mean of the noise given by $E\big(w'(n)\big) = a_3 i_L(n-1)$ and the variance of $w'(n)$ is given by the variance of the process noise $\sigma_w{}^2$. Similarly the scalar observation equation for the Kalman filter can be obtained by considering only the change in capacitor voltage and by modeling the change in inductor current along with noise. Hence, (3.10) can be modified as given below:

$$v_0(n) = c\, v_c(n) + v'(n) \tag{3.14}$$

where,$v'(n)$ is white Gaussian noise with variance equal to $\sigma_v{}^2$. The mean of the noise is given by

$$E\big(v'(n)\big) = c' i_L(n-1) \tag{3.15}$$

The Kalman filter is a recursive filter and let $\widetilde{v_c}((n-1)/(n-1))$ denote the best estimate of $v_c(n-1)$ obtained from the Kalman filter up to $(n-1)$ observations. The estimate of $v_c(n)$ predicted by the small signal model obtained from (3.11) and (3.12) is given below:

$$\widetilde{v_c}(n/(n-1)) = a_4\widetilde{v_c}((n-1)/(n-1)) + a_3 i_L(n-1) \tag{3.16}$$

For 'n' given observations (n is an integer number) of $v_0(i)\{\text{for } i = 1,2 \ldots . n\}$, the best estimate of $v_c(n)$ is obtained using Kalman filter, which can be expressed as given below:

$$\widetilde{v_c}(n/n) = \widetilde{v_c}(n/(n-1)) + k(n)(v_0(n) - c' i_L(n-1) - c\widetilde{v_c}(n/(n-1))) \tag{3.17}$$

where $k(n)$ is the Kalman gain, $\widetilde{v_c}(n/n)$ denote the best linear estimate of $v_c(n)$

The Kalman gain $k(n)$ is computed as follows

$$k(n) = \frac{P(n/(n-1))c}{c^2 P((n-1)/(n-1)) + {\sigma_v}^2} \tag{3.18}$$

where, $P(n/(n-1))$ is the minimum prediction mean square error for $(n-1)$ observations and it is given by

$$P(n/(n-1)) = {a_4}^2 P((n-1)/(n-1)) + {\sigma_w}^2 \tag{3.19}$$

The minimum mean square error estimation for n observations is given by

$$P(n/n) = ((1 - k(n)c)P(n/(n-1)) \tag{3.20}$$

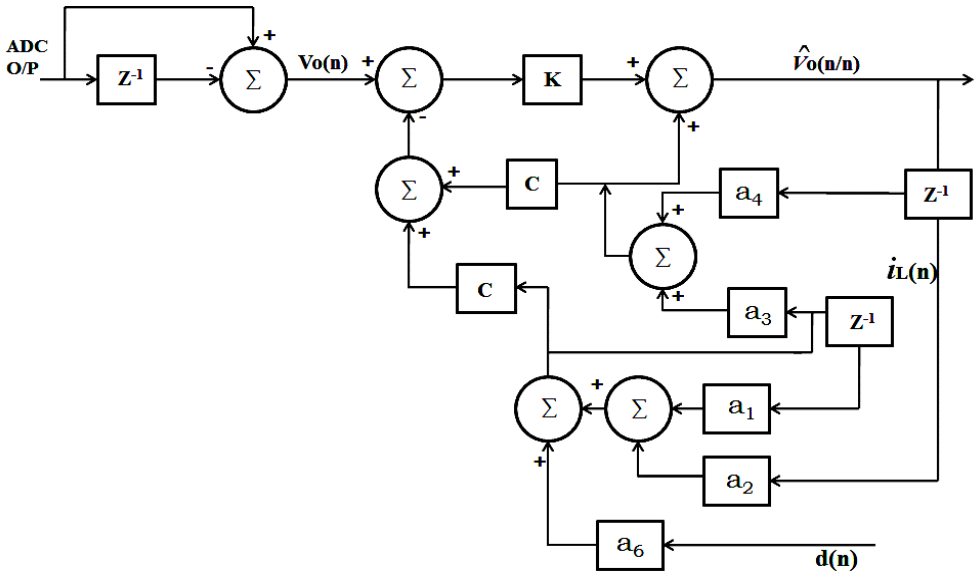

Figure 3.2: Block diagram of the scalar state scalar observation Kalman filter

If the system is modeled with two state variables, the computational effort associated with matrix inversion is $O(n^3)$, and matrix multiplication is $O(n^2)$, where n is the number of states of the system [63]. Due to the implementation of the reduced state Kalman filter and offline computation of Kalman gain, three algebraic equations given in (3.3), (3.16) and (3.17) are only required for estimating the optimum value of capacitor voltage. These algebraic equations require simple additions and multiplications for the implementation. Therefore, the implementation of the Kalman filter does not introduce more phase delay as the execution of these three equations takes minimum clock cycle, and will not affect the phase margin of the converter.

3.4. Simulation result

A mathematical model of the digitally controlled buck converter is used to compute the Kalman gain. The converter parameters used for the modeling are $L = 100\ \mu H$, $C=22\ \mu F$, $R_C = 0.1\ \Omega$, $R = 2.5\ \Omega$, $R_L = 0.025\ \Omega$, $Vin = 12$ to $18\ V$ and $Vout = 5\ V$. In this model sampling period is chosen as same as switching frequency ($T_s = 2.5\ \mu sec$).

3.4.1 Closed loop model

The discrete time transfer function $G_{0L}(z)$ of the overall open loop system is derived by adopting the modeling approach presented in [20] and [23]. The overall open loop system $G_{0L}(z)$ comprises of the power stage, Zero order hold, ADC gain, feedback factor, DPWM gain and the total computational delay in the control loop. The Simulink model of the buck converter with Kalman filter is given in Figure 3.3.

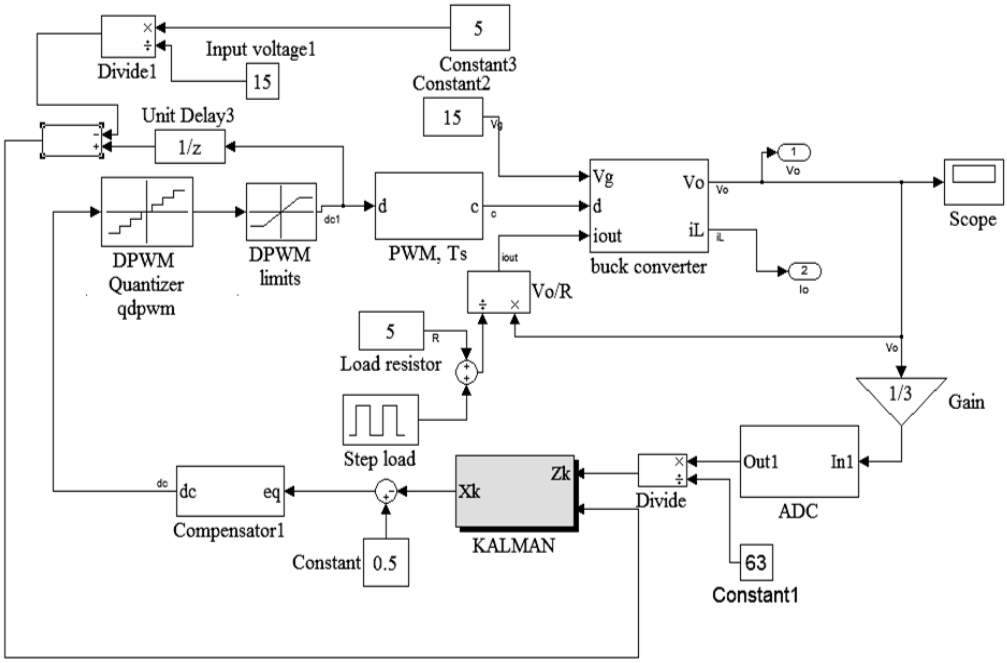

Figure 3.3a: Simulink model of the DC-DC converter with Kalman filter

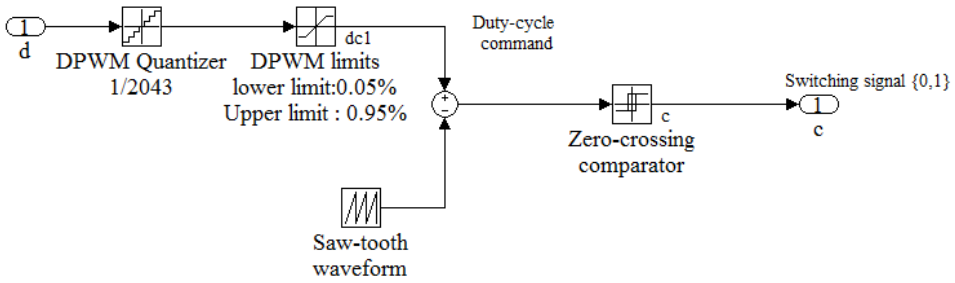

Figure 3.3b: Simulink model of the DPWM

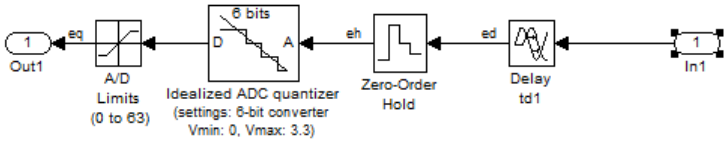

Figure 3.3c: Simulink model of the ADC

For the buck converter the small signal output voltage to the PWM duty ratio (control to output transfer function), $\frac{V_0}{d}$, is expressed as $G_p(s)$ and is given by

$$G_P(s) = \frac{V_{in}(sR_cC+1)}{s^2LC\frac{R_L+R_c}{R_L}+s\left(\frac{R_cC(R+R_L)}{R_L}+\frac{L}{R_L}+RC\right)+\frac{R+R_L}{R_L}} \tag{3.21}$$

The ADC is modeled with the gain, sample and hold and conversion time. The gain of the ADC is given by

$$k_{adc} = \frac{2^{n_{adc}} - 1}{3.3} \tag{3.22}$$

where n_{adc} is the resolution of the ADC. The operating voltage range of the ADC is from 0 to 3.3 V.

The zero order hold is given by

$$SH(s) = \frac{1 - e^{-sT_s}}{s} \tag{3.23}$$

where T_s is the sampling period.

The delay block in Figure 3.3 models the total delay in the loop. The total time delay (td) is the time between the ADC sampling instant and the subsequent PWM duty ratio update. The delay includes ADC conversion time and the computation delay. It is expressed as

$$Gdly(s) = e^{-std} \tag{3.24}$$

The gain of the DPWM block is given by

$$k_{dpwm} = \frac{1}{2^{n_{dpwm}} - 1} \tag{3.25}$$

where $n_{dpwm}$is the resolution of the DPWM.

The transfer function of overall open loop system including the power stage, feedback gain, FB, gain of ADC, Sample & hold and gain of DPWM and the computation delay can be expressed as

$$G_{OL}(s) = G_p(s)\, Gdly(s)\, k_{adc}\, k_{dpwm}\, SH\, FB \tag{3.26}$$

The continuous time model given in equation (3.26) is converted to discrete time model with sample time T_s by using MATLAB. The sampling period is same as that of the switching frequency. The discretization method uses the zero order hold on the inputs. The discrete time open loop transfer function is given by

$$G_{0L}(z) = \frac{0.006426z + 0.003682}{z^2 - 1.953z + 0.9555} \tag{3.27}$$

The computational delay is chosen as $0.5\, T_S$.

A suitable controller $G_c(z) = \frac{1.7309(z-0.974)(z-0.9463)}{(z-1)(z-0.7521)}$ is designed to compensate the system $G_{0L}(z)$ in such a way that the gain rolls off at a slope of –20dB/decade at 0 dB. The bandwidth of system is selected as 5 kHz to ensure no limit cycle oscillation with a phase margin of greater than 45 degrees. The open loop bode response of the converter with controller up to the Nyquist frequency of 200 kHz ($\frac{f_{sw}}{2}$, where f_{sw} is the switching frequency) is given in Figure 3.4 and it is observed that the compensator design is meeting with a bandwidth of about 5 kHz and a phase margin of greater than 45 degrees. The above designed controller works very well with a Kalman filter in the loop, as it introduces only very less computational delay in the control loop. Since the Kalman filter is implemented using three algebraic equations, the computational delay is significantly low and will not affect the stability of the loop. Moreover, the assumption of additional $0.5\, T_S$ for the total delay in the loop while designing the controller, accounts for the execution time of the Kalman filter.

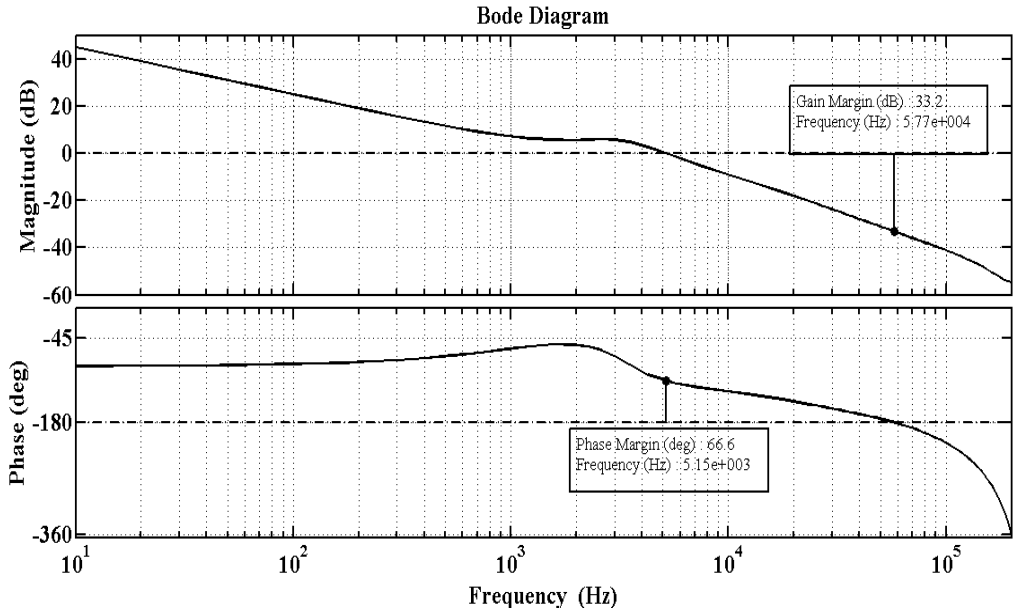

Figure 3.4: Bode response of the plant with controller

3.4.2 Computation of Kalman gain

Based on the converter parameter, (3.8) can be rewritten and is as follows:

$$\begin{bmatrix} i_L(n) \\ v_c(n) \end{bmatrix} = \begin{bmatrix} 0.9957 & -0.02347 \\ 0.1067 & 0.956 \end{bmatrix} \begin{bmatrix} i_L(n-1) \\ v_c(n-1) \end{bmatrix} + \begin{bmatrix} -0.00382 \\ 0 \end{bmatrix} v_g(n-1) + \begin{bmatrix} 0.6849 \\ 0 \end{bmatrix} d(n-1) \quad (3.28)$$

The Kalman gain is computed offline using the MATLAB model which uses equation (3.18), (3.19) and (3.20). The design guideline for the computation of Kalman gain is given in Appendix 2. The measurement error is due to the quantization of ADC and its variance for 6 bit ADC is $2.255 * 10^{-4}$. To compute the process noise error variance, [66], [67] and [68], the two noise sources due to the quantization of ADC and DPWM are injected into the feedback system at the corresponding point and its effect on the output voltage is obtained. The noise injected by ADC has a mean square noise of $\frac{{q_{adc}}^2}{12}$ and the noise injected by DPWM has a mean square noise of $\frac{{q_{dpwm}}^2}{12}$. The impulse response from the point of

injection of each noise to the output is computed. Also the sum of squares of the impulses of the impulse response from the quantizer to system output is determined. The variance of the quantization noise at the system output due to the ADC quantizer is $\frac{{q_{adc}}^2}{12}$ multiplied by the sum of the squares of the impulses of the impulse response from the quantization point to system output [64]. Similarly, the variance of the quantization noise at the system output due to DPWM is calculated. The sum of the individual variance of ADC and DPWM is the variance of the total quantization noise at the system output. Thus, the process noise variance computed by taking the quantization effect of 6 bit ADC and 11 bit DPWM for a reference voltage of 1.6405V is $1.855 * 10^{-3}$. Using these two parameters, the Kalman gain computed is 0.9271, for the input voltage of 18 V. Under conditions where process noise variance and measurement noise variance are constant, both the estimation error variance P(n) and the Kalman gain k(n) will stabilize quickly and then remain constant as shown in Figure 3.5. Hence the Kalman gain k(n) can be computed offline facilitating the computationally efficient realization of the Kalman filter.

It may be noted that the Kalman gain remains the same even if the input voltage changes from 12 V to 18 V as the state vector for the converter is invariant. However, the gain can vary as the load changes from minimum to maximum load condition. To assess the effect of the state reduction on the Kalman gain, the Kalman gain is computed by using the vector state model of the converter. The Kalman gain computed is $[-0.0009\ 0.9272]$.This shows that the Kalman gain is very close to the previously computed value of 0.9271.

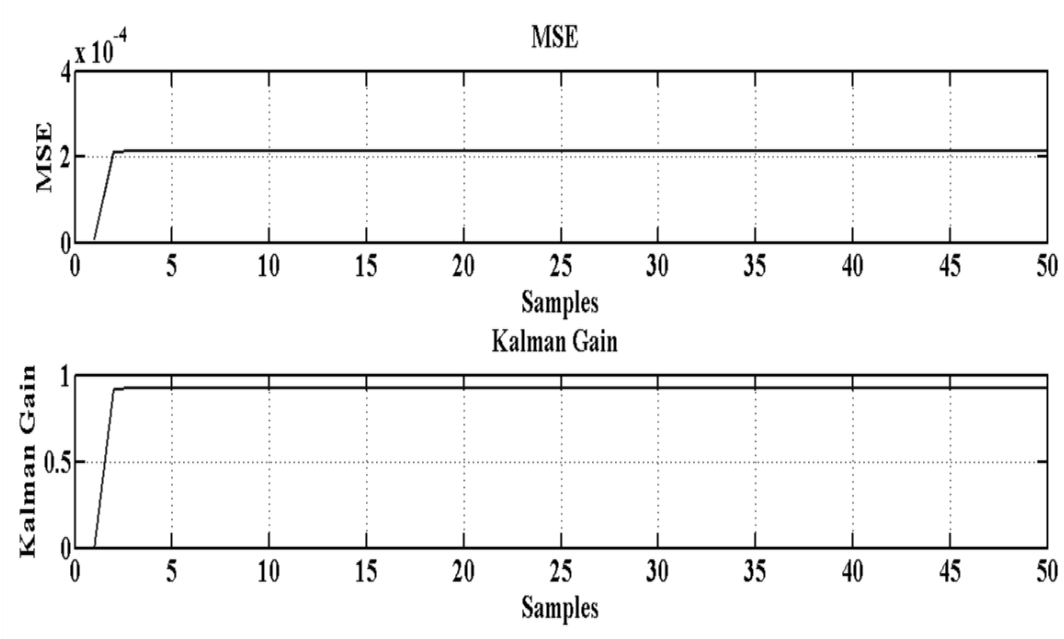

Figure 3.5: Mean square error and Kalman gain for 6-bit ADC and Vref: 1.6405 V

3.4.3 Results

The simulated output voltage response obtained from the model with Kalman and without Kalman filter for a 6-bit ADC is shown in Figure 3.6. The results show that the proposed scheme brings considerable reduction in the limit cycle oscillation (around 100 mV) at the output of the converter. In practice, the limit cycle oscillations will be more as the modeling has not considered the round off errors and finite word length of fixed point DSP processors.

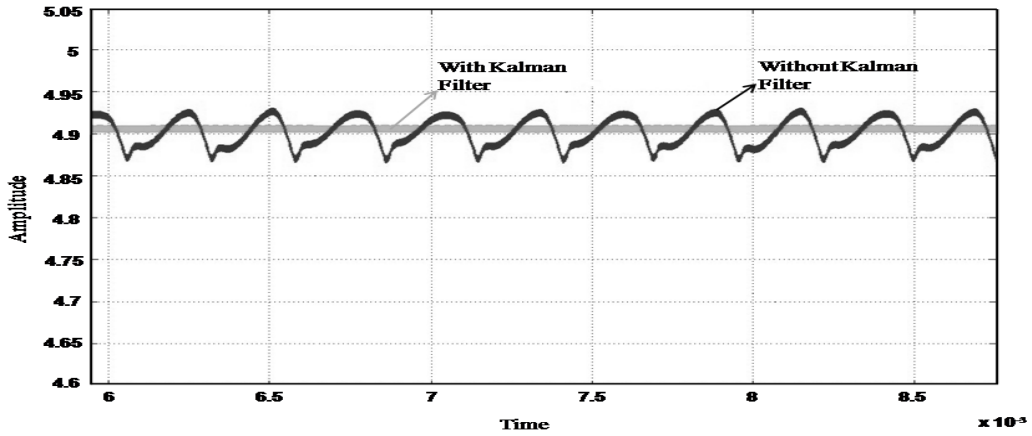

Figure 3.6: Output voltage response with and without Kalman (X axis: 6.125×10^{-3} to 8.75×10^{-3} sec, X axis scale:0.5×10^{-3} sec, Y axis: 4.6 to 5.05 V, Y axis scale:0.05 V)

3.5 Experimental results

The prototype model of the digitally controlled buck converter is implemented to verify the effectiveness of the proposed reduced state Kalman filter. The converter is realized with the following specifications: i) Input voltage range 12-18 V ii) Output voltage 5 V iii) Minimum and maximum load current of 200 mA and 2 A iv) Line regulation, load regulation and ripple is set as 1 %, 1 % and 50 mV respectively v) Switching frequency of the converter 400 kHz.

The circuit diagram of the hardware is shown in Figure 3.7. The circuit is realized using surface mount devices in a PCB card dimension of 8x4 cm. Fast switching MOSFET (IRFN240) has been used as the switching element, U1, in the power stage and the buck converter comprises of output inductor, L1, 100 µH, SMP 5022 of M/S Gowanda and the output capacitor, C2, is 22 µF with ESR of 100 mΩ, CWR09KC226JDC type. These values are designed based on the equations (1.5) and (1.6). A bank of capacitors is also provided at the output. The bank of capacitors comprises of C3- 0.1 µF, C4- 0.01 µF and C5-1000 pF. C3 is of CDR 33 type, whereas C4 and C5 are of CDR32 type. The controller, U4, is implemented using 16-bit digital signal controller, dsPIC33FJ16GS502 of Microchip Technology Inc. A Power on Reset (POR) is provided during initial power on. The POR circuit comprises of capacitor C18, 10 µF in parallel with C17, 0.01 µF, CDR 33 type. The charging path is through R10, 10 kΩ resistor so as to provide a POR time of 85msec. The diode D3, 1N5811USJANTX, is provided for the discharge path of C18. The 3.3 V supply for dsPIC is derived using LT1963, U2, a fast transient response LDO regulator. In order to reduce the thermal dissipation in LT1963, a simple emitter follower series pass regulator comprising of Q1, Z1 (1N748JTX), R6 (1K) and R7 (100 Ω parallel 100 Ω), is used to derive 6.5 V from the input voltage. This is further dropped to 4.89 V by using the parallel resistors R8 and R9 (47 Ω parallel 47 Ω) before giving it to the input of LT 1963. The PWM output from the dsPIC is given to IR2110, U3. IR2110 is a high voltage, high speed power MOSFET driver with independent high and low side referenced output channels. Gate drive supply voltage can range from 10 to 20 V. Hence the supply for this IC is derived directly from the input voltage.

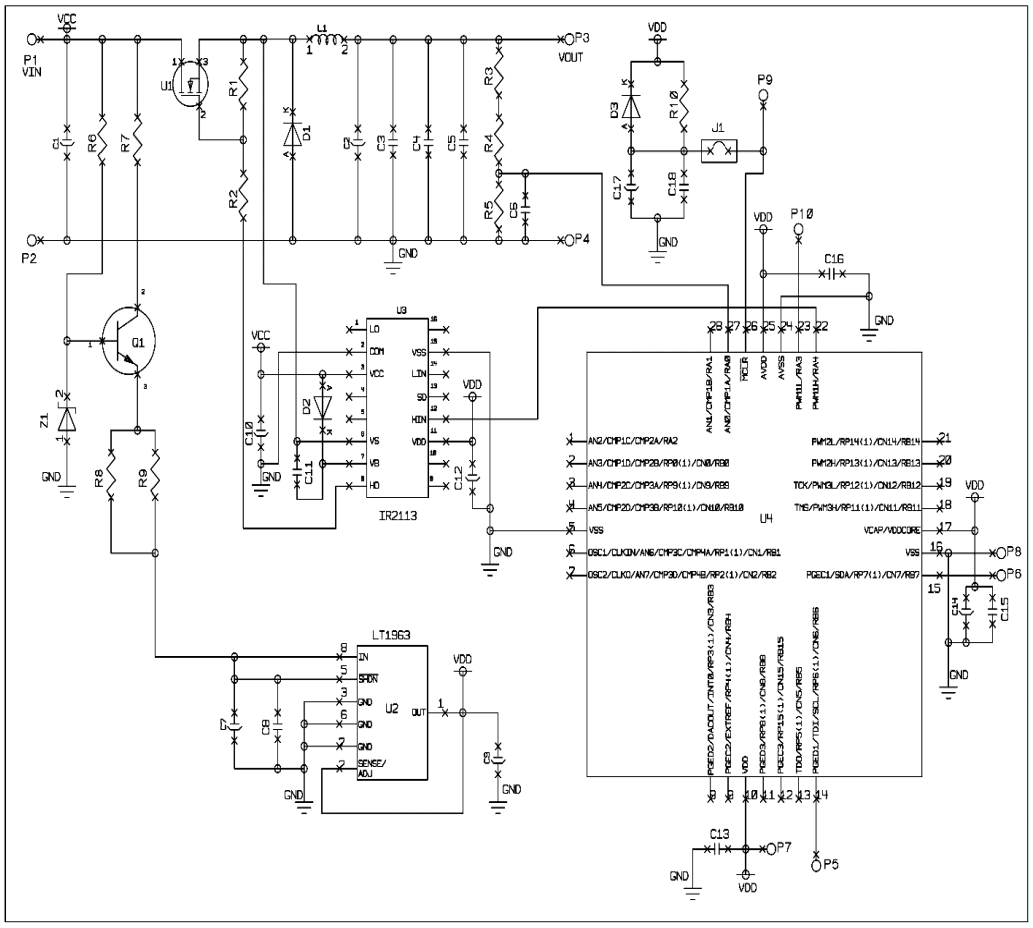

Figure 3.7: Circuit diagram of the implemented hardware

The dsPIC33FJ16GS502 is a 28 pin device with QFN-S package. This chip is of CMOS Flash technology with operating speed of 40MIPS. It has program memory of 16 kbytes, RAM of 2 kbytes, three 16 bit Timers, ADC with 10bit resolution with up to two Successive Approximation Register converters (4 Msps) and up to six Sample and Hold circuits and four PWM outputs with 1.04 ns resolution. It has a Code efficient (C and Assembly) architecture with two 40 bit wide accumulators, Single cycle (MAC/MPY) with dual data fetch, Single cycle mixed-sign MUL plus hardware divide and 32 bit multiply support. For clock management, it has internal oscillator, Programmable Phase Locked Loop (PLL) and oscillator clock sources. It has Fail Safe Clock Monitor, Independent Watchdog Timer, Fast Wake-up and Start up features. The communication interfaces include UART module, 4 wire SPI module and I^2C module. The general block diagram of the peripheral and core module of the processor is given in Figure 3.8.

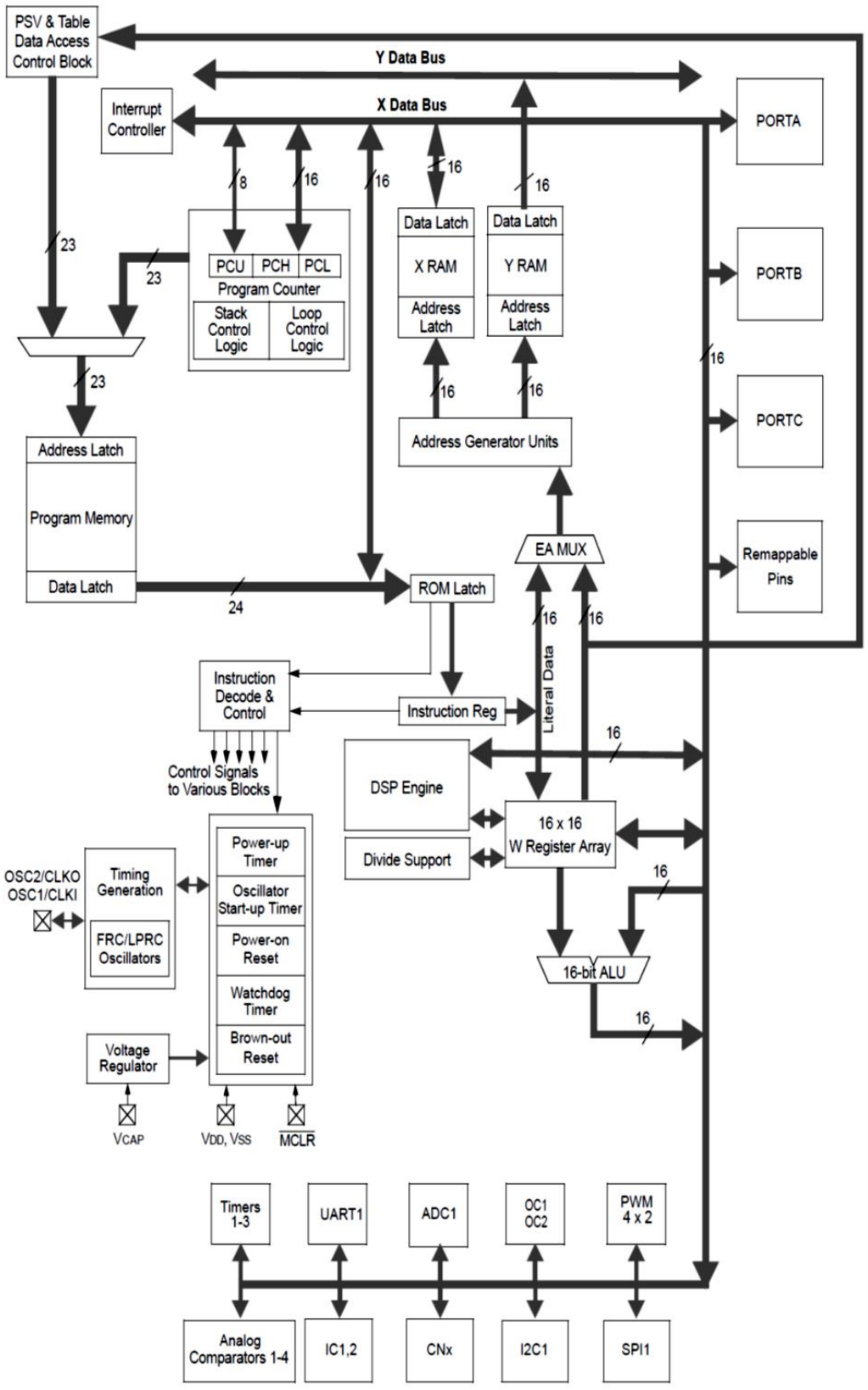

Figure 3.8: Block diagram of the core and the processor modules

The oscillator source used at the device power on reset event is selected using the configuration bit settings. The oscillator configuration bit settings are located in the configuration registers in the program memory. In this work, the internal fast RC oscillator is used with PLL so that the dsPIC operates at full speed. The fast RC oscillator runs at a nominal speed of 7.37 MHz. The internal RC oscillator is given to a PLL as shown in Figure 3.9. The output of the primary oscillator is divided by a pre scale factor of two. Thus the input of the Voltage Controlled Oscillator (VCO) is 3.685 MHz. The input of the VCO is multiplied by a factor M so that the processor operates at the maximum clock speed. In this design, M is selected as 41 so that F_{vco} is 158.455 MHz. The VCO output is further divided by two so that the device operating frequency is 79.225 MHz. The oscillator frequency (F_{osc}) is divided by two to get the operating frequency, F_{CY} or instruction execution speed.

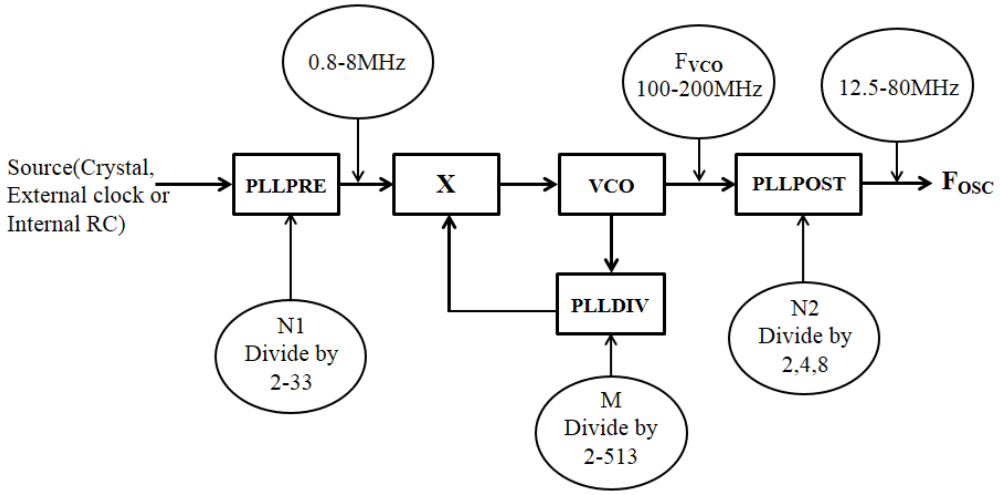

Figure 3.9: Oscillator portion of the dsPIC

An auxiliary clock generation is used for PWM and ADC that is unrelated to the system clock. An auxiliary PLL is used to obtain the auxiliary clock, which is having a fixed multiplication factor of 16. Thus the auxiliary clock frequency is 117.92 MHz. Standard edge aligned PWM is chosen for generating the PWM. To create the edge aligned PWM, a timer or counter circuit counts upward from zero to a specified maximum value, called the 'period'. Another register contains the

duty cycle value, which is constantly compared with the timer (period) value. When the timer or counter value is less than or equal to the duty cycle value, the PWM output signal is asserted. When the timer value exceeds the duty cycle value, the PWM signal is de-asserted. When the timer is greater than or equal to the period value, the timer resets itself, and the process repeats. Figure 3.10 shows the standard edge aligned PWM.

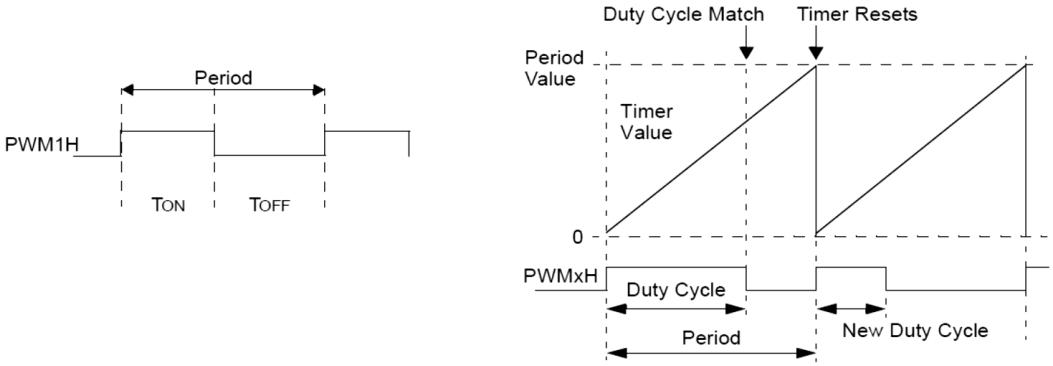

Figure 3.10: Standard edge aligned PWM

The PWM period value defines the switching frequency of the PWM pulses. The PWM period value is controlled by the Phase Shift registers, PHASEx and the PHASEx has to be loaded as per the equation given in the data sheet of dsPIC.

Since the objective is to reduce the resolution of ADC and to achieve better limit cycle specification, the ADC is configured for 6-bit resolution and DPWM is configured for 11 bits. The ADC has analog input range of 0 to 3.3 V and the conversion time is approximately 600ns. The ADC samples the scaled down output voltage at the center of the switching period so as to avoid sampling at the switching spikes of output voltage. If the output voltage is within the range of 4.5 V and 5.5 V, ADC output is fed to Kalman filter else it is fed to the digital controller directly.

The coefficients of the controller are first converted to a suitable fixed point format (Q format) in order to get the best accuracy out of this 16-bit processor. Since the largest value of integer portion of coefficients is 1.732, a maximum of four bits will be sufficient to represent the signed integer. So pre-computed PID co-efficient, the parameters of the small signal model and Kalman gain are stored in Q12 format of fixed point representation. The reference voltage is given in Q14 format. The output of the ADC is converted to Q14 format and the format used for representing the

error signal is Q14. The two sample old and one sample old error signal is also stored in Q14 format. In the PID controller the multiplication of a Q14 format number by a Q12 number results in a Q26 format number and it is stored in a 32-bit register. Since the higher 16 bits of the result is extracted, and it is left shifted by four to give the result of multiplication in Q14 format. The result, i.e., the output signal of PID controller after the execution of above algebraic equation is stored in Q15 format. As far as memory is concerned, the data memory requirements for storing the constants are very much dependent on the order of the compensator and the data word length used. Here the data word length used to represent the constants and variables are 16 bit. Hence the total data memory required to store the coefficients of the PID controller and the other converter related constants are 24 bytes (12 × 16 bits). The total program memory used for the implementation of the above algorithm in dsPIC33FJ16GS502 is around 854 bytes. The Kalman filter is implemented with 35 instruction cycles based on the proposed state reduction with offline computation of Kalman gain. Coding was done in assembly language. The prototype model of the system with proposed reduced Kalman filter is shown in Figure 3.11 and the flowchart of the program is given in Figure 3.12.

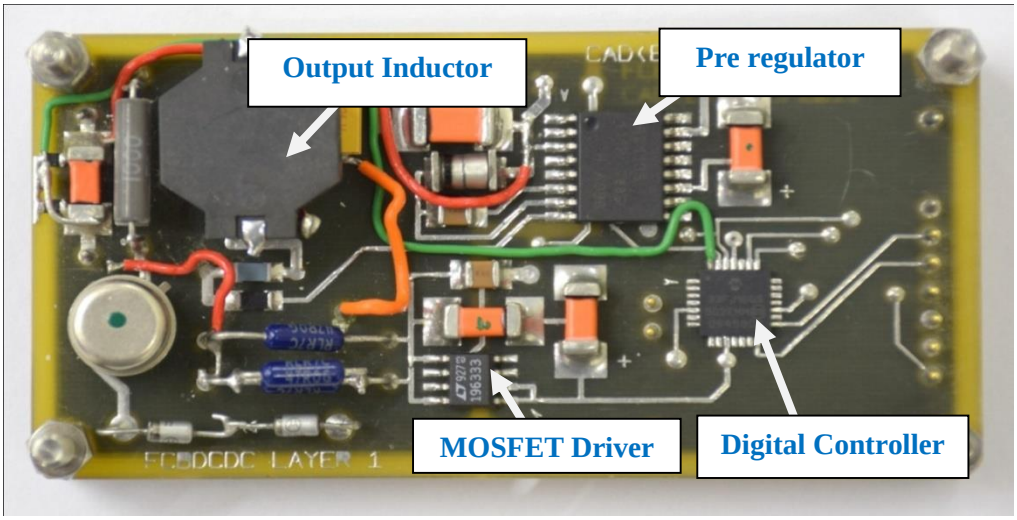

Figure 3.11: Prototype set up of the proposed scheme

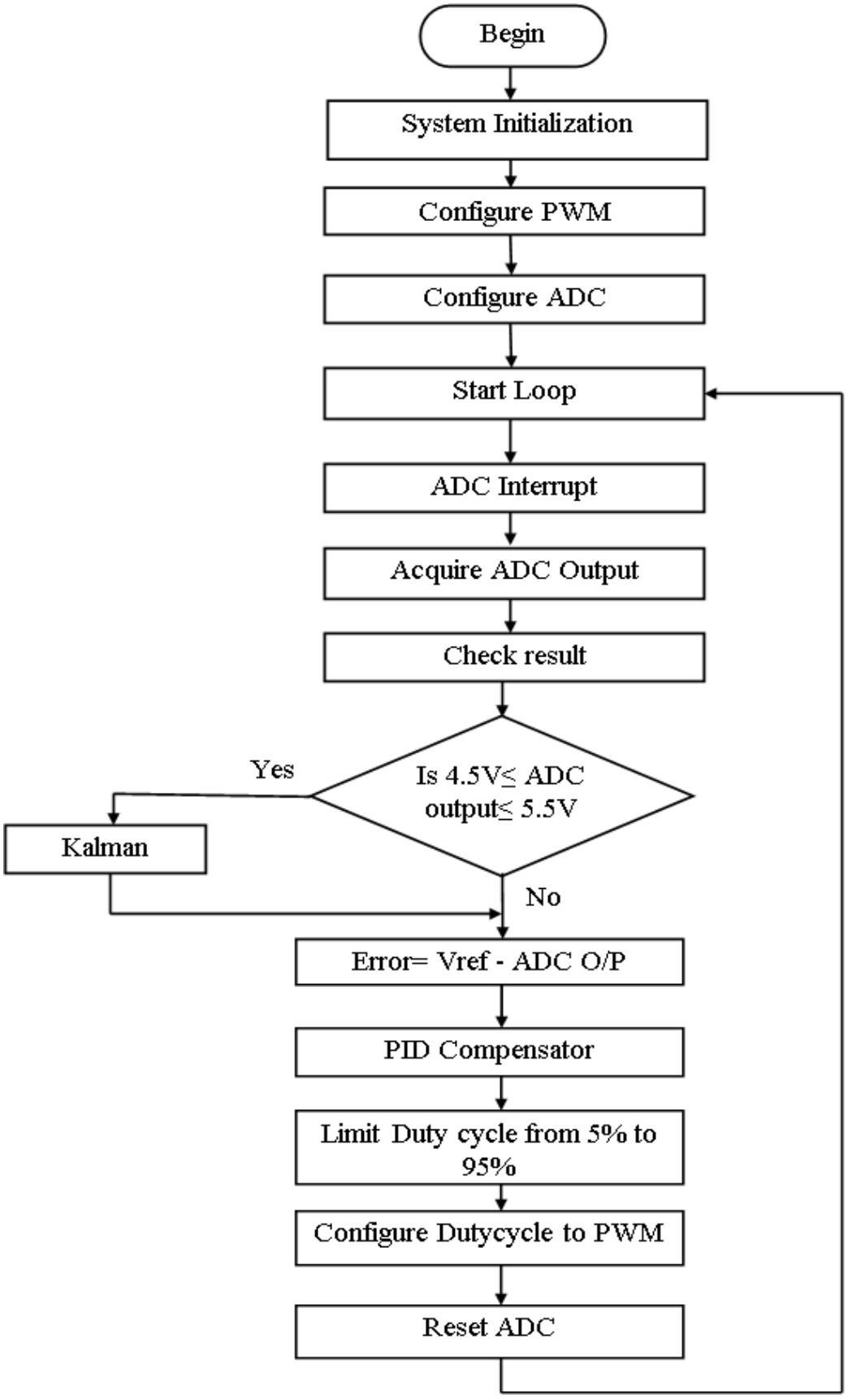

Figure 3.12: Flowchart of the controller implementation in dsPIC

The programming of dsPIC33FJ16GS502 is done by using the pins PGED1: Data input/output pin for programming, PGEC1: Clock input for programming, MCLR: Master Clear (Reset) input, VDD: Positive Supply and VSS: Ground. These pins are made available at pads. During programming, these pins are connected to programmer (ICD3) and program is loaded using MPLAB IDE software.

Figure 3.13a shows the output of the converter with 6-bit ADC without Kalman filter scheme. The reference voltage is fixed at 1.65 V so that the output voltage exactly coincides with quantization level and thereby resulting in no limit cycle oscillations. The ripple is within specification (around 20 mV at 400 kHz) and respective FFT of the output voltage is shown in Figure 3.13b.

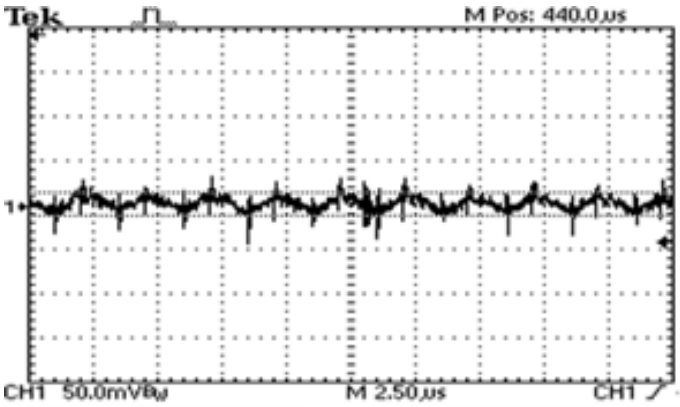

Figure 3.13 a

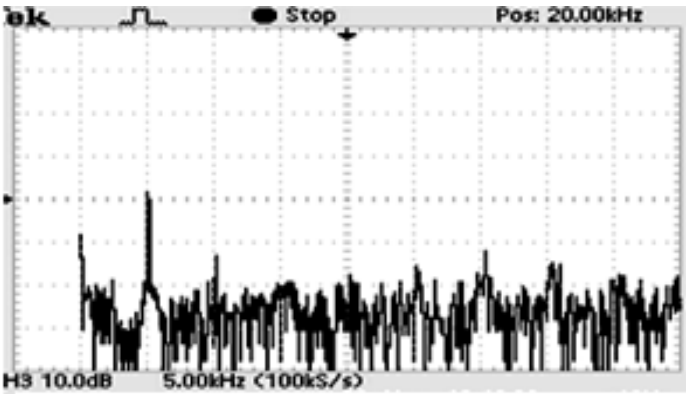

Figure 3.13b

Figure 3.13: Converter output (AC coupling mode of oscilloscope) (3.13a) and FFT of the output (3.13b) with 6 bit ADC & without Kalman (Vref: 1.65 V) (Fig: 3.13b x axis: Frequency (kHz) , x axis scale : 5 kHz and y axis: Amplitude in dB, y axis scale: 10 dB)

To study the effect of the reference voltage of the converter, small change in magnitude is introduced (1.6405 V), which is shown in Figure 3.14a. From the figure it is observed that the limit cycle oscillation has increased to 600 mV with frequency of around 4.16 kHz. The large amplitude of limit cycle oscillation is due to the fact that the reference voltage is such that the output of the converter does not fall within the quantization levels of ADC. The increase in amplitude of the limit cycle is confirmed by taking the FFT of the limit cycle at the converter output which indicates the component near 4.16 kHz as shown in Figure 3.14b.

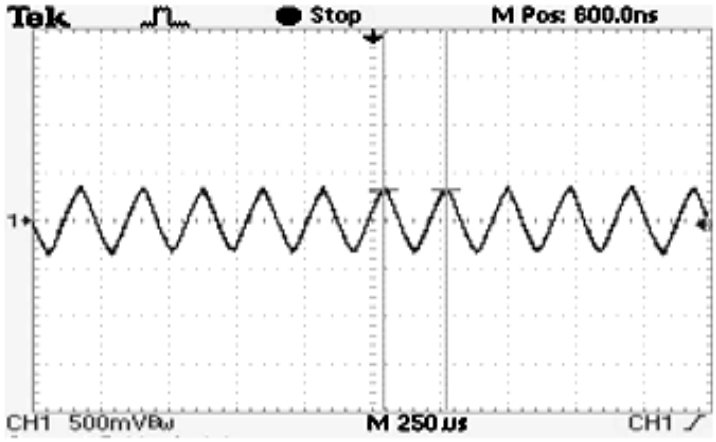

Figure 3.14a

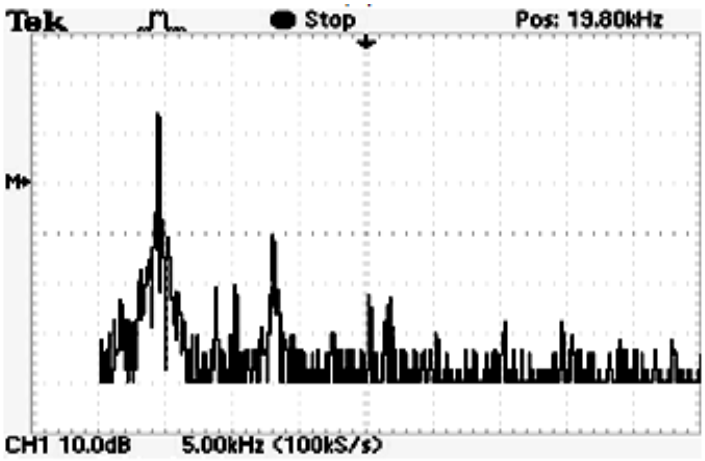

Figure 3.14b

Figure 3.14: Converter output (AC coupling mode of oscilloscope) (3.14a) and FFT of the output (3.14b) with 6 bit ADC & without Kalman filter (Vref: 1.6405V) (Fig: 3.14 b x axis: Frequency (kHz), x axis scale: 5 kHz and y axis: Amplitude in dB, y axis scale:10 dB)

Further the output of the ADC is processed using a Kalman filter. Here, the Kalman gain is set as 0.92, which is computed offline. It can be seen from Figure 3.15a that the limit cycle voltage is less than 50 mV (around 20 mV) with frequency of 400 kHz. Figure 3.15b shows the FFT of the output voltage with considerable reduction in limit cycle (30 dB). The experiment is repeated by varying the line voltage from 12 to 18V with the load variation of 200 mA to 2 A and it is observed that the line regulation and load regulation is well within the specification of 1 %. Thermal test is also carried out to confirm that the offline computed Kalman gain works for the operating temperature range of 8°C to 70°C satisfactorily.

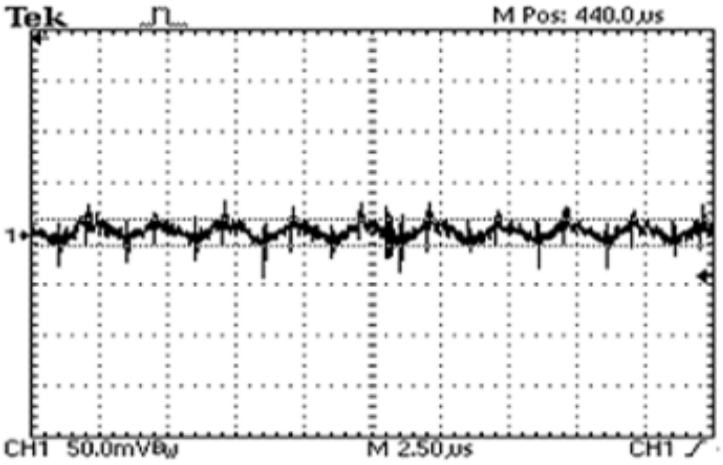

Figure 3.15a

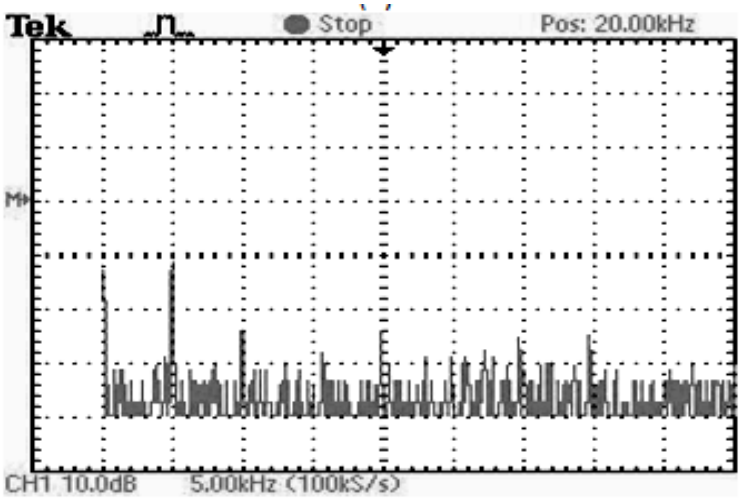

Figure 3.15b

Figure 3.15: Converter output (AC coupling mode of oscilloscope)(3.15a) and FFT of the converter output (3.15b) with 6 bit ADC & with Kalman filter (Vref:1.6405V)

The experiment is repeated (without Kalman filter) for reference voltage of 1.625V and limit cycle oscillation of amplitude 340 mV at 3.486 kHz is observed which is shown in Figure 3. 16a.The output of the converter (with Kalman gain of 0.875) with significant reduction in limit cycle amplitude is shown in Figure 3.16b. The ripple frequency is at 400 kHz and amplitude is 20 mV.

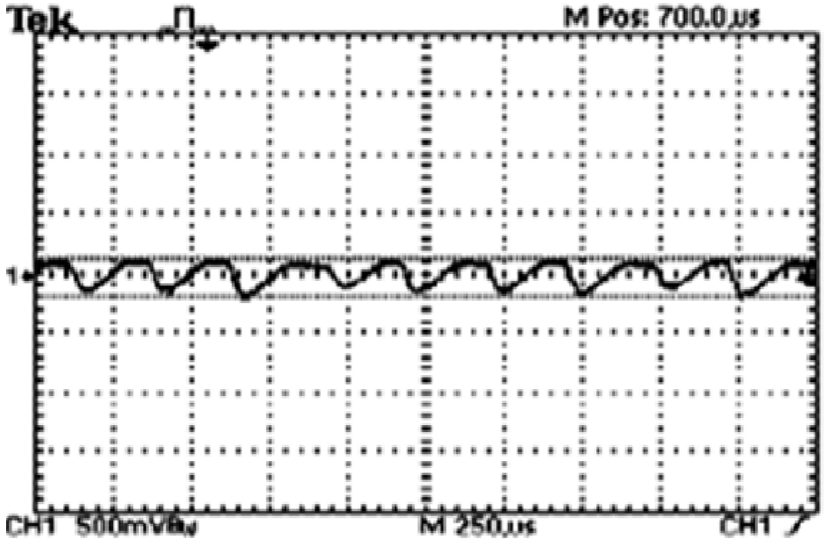

Figure 3.16a

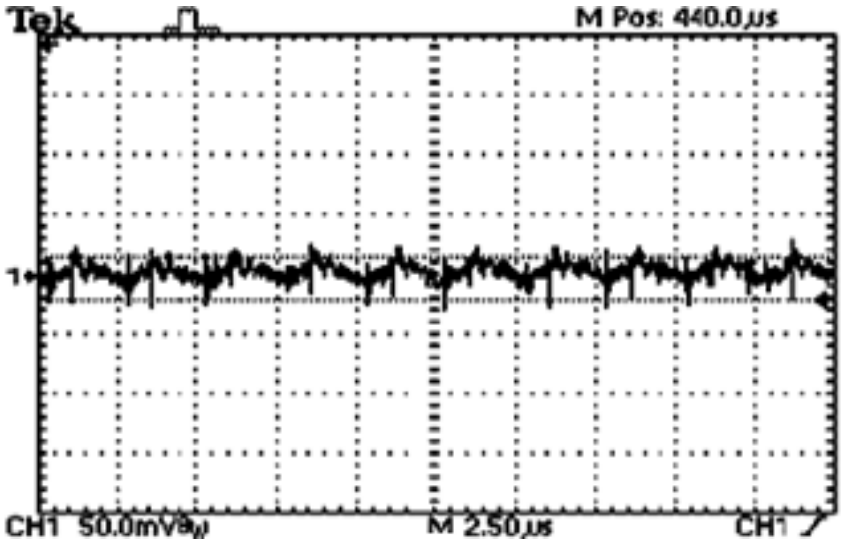

Figure 3.16b

Figure 3.16: Converter output (AC coupling mode of oscilloscope) with 6 bit ADC without Kalman (3.16a) and with Kalman filter (3.16b) (Vref: 1.625 V)

The limit cycle oscillation, at the output of the converter, without Kalman filter in the case of 5-bit ADC with reference voltage of 1.596 V is shown in Figure 3.17a. The limit cycle oscillation is of 800 mV at around 4 kHz. Figure 3.17b shows that limit cycle oscillation has been significantly reduced with Kalman filter having the filter gain of 0.83. The ripple frequency is at 400 kHz and amplitude is 20 mV.

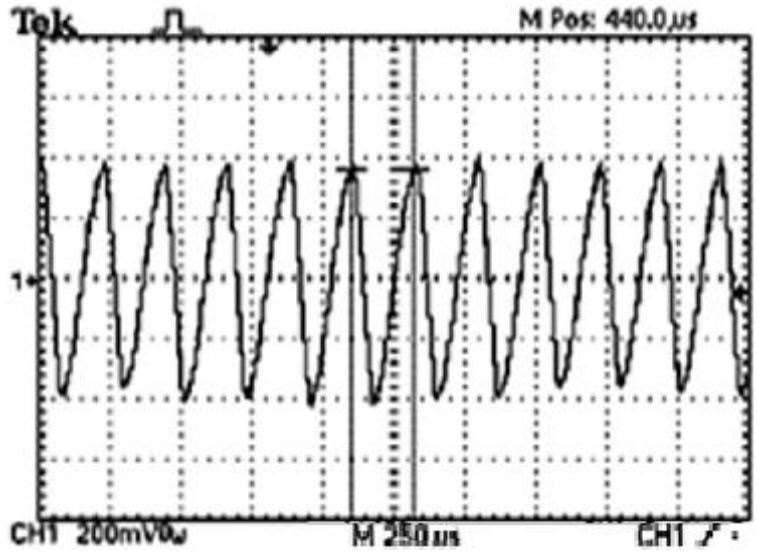

Figure 3.17a

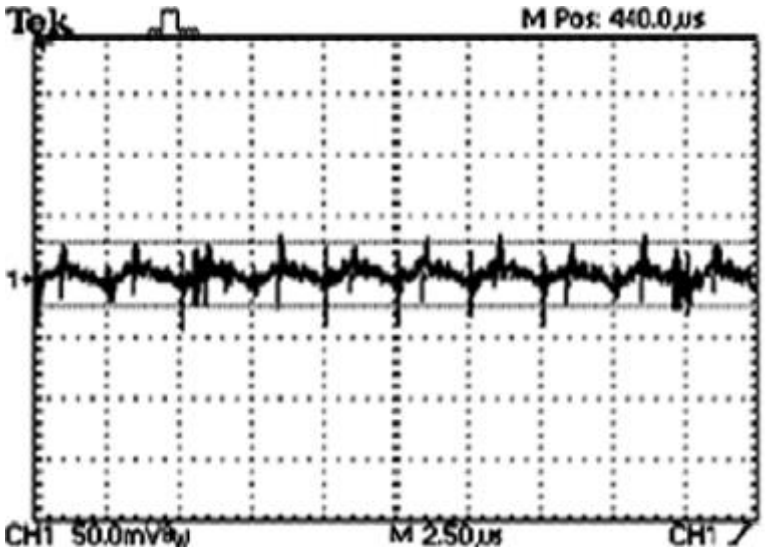

Figure 3.17b

Figure 3.17: Converter output (AC coupling mode of oscilloscope) with 5 bit ADC without Kalman (3.17 a) and with Kalman filter (3.17 b) (Vref: 1.596 V)

The experiment is repeated again by changing the ADC resolution from 8 bit to 4 bit for the reference voltage of 1.596 V. The Kalman gain used for the experiment is summarized in Table 3.1 and it is found that the Kalman gain in each case is different as the measurement noise error variance and process noise error variance are different. The amplitude of the limit cycle oscillation at the output of the converter without Kalman filter and with Kalman filter is also tabulated in Table 3.1. It is found that in all these cases the limit cycle oscillation has been significantly reduced. The proposed scheme is found to be effective up to 4-bit resolution of ADC.

Table 3.1. Kalman gain and limit cycle oscillation for different resolutions of ADC

V_{ref}:1.596 V			
Resolution of ADC	Kalman gain	Limit cycle oscillation without Kalman filter	Limit cycle reduction with reduced Kalman filter
8	0.95	200 mV at 4.23 kHz	<50mV 400kHz (switching frequency)
7	0.9648	300 mV at 3.788 kHz	
6	0.8125	880 mV at 4.2 kHz	
5	0.83	800 mV at 4 kHz	
4	0.8125	60 mV at 3.788 kHz	

The transient response of the converter is taken to study the effect of introduction of Kalman filter on the stability margins. It is found that there is no considerable variation in the transient response which confirms that the stability margins are not affected by introduction of Kalman filter. Figure 3.18a and Figure 3.18b shows the transient response of the converter, without Kalman and with Kalman filter respectively when the load changes from 50 to 100 % of the maximum load. The output of the converter (5 V) is captured in the AC coupling mode of the oscilloscope. From Figure 3.18a and Figure 3.18b, it is noted that the overshoot is less than 17%, which indicates that the phase margin is more than 45º. It is found that the proposed scheme of state reduction and offline computation of Kalman gain

has effectively reduced the computational time and has not introduced any phase lag.

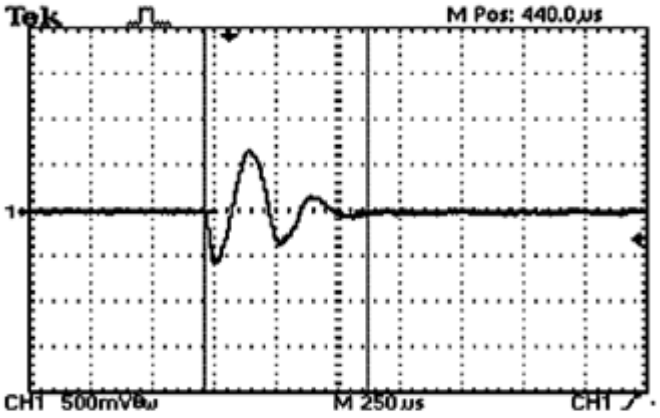

Figure 3.18a

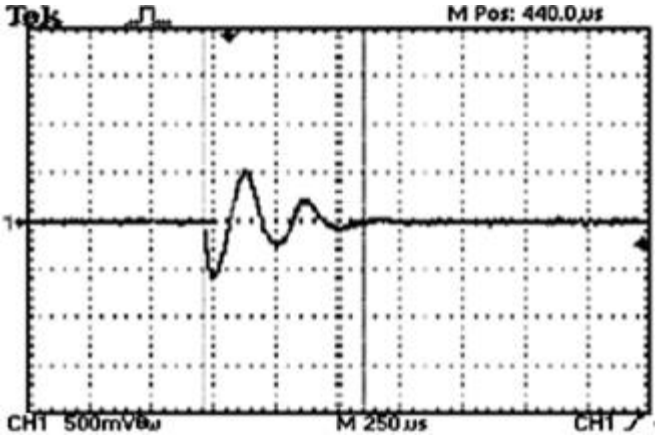

Figure 3.18b

Figure 3.18: Transient response of the converter (AC coupling mode of oscilloscope) for 6 bit ADC without Kalman (3.18a) and with Kalman filter (3.19b) (Vref: 1.67 V)

The CS01 test of MIL STD 461C was conducted on the package to check whether the introduction of Kalman filter in the loop has affected the audio susceptibility. The CS01 test measures the conducted susceptibility in the frequency range of 30 Hz – 50 kHz on the input power lines. The injected amplitude of the audio frequency is nearly 1.5 Vrms for input voltage of 15 V (10 % of input voltage) for frequencies below 1.5 kHz and the amplitude decreases linearly to 0.5 Vrms at 50 kHz. The audio signal is superimposed on the DC input voltage as shown in the test set up of Figure 3.19.

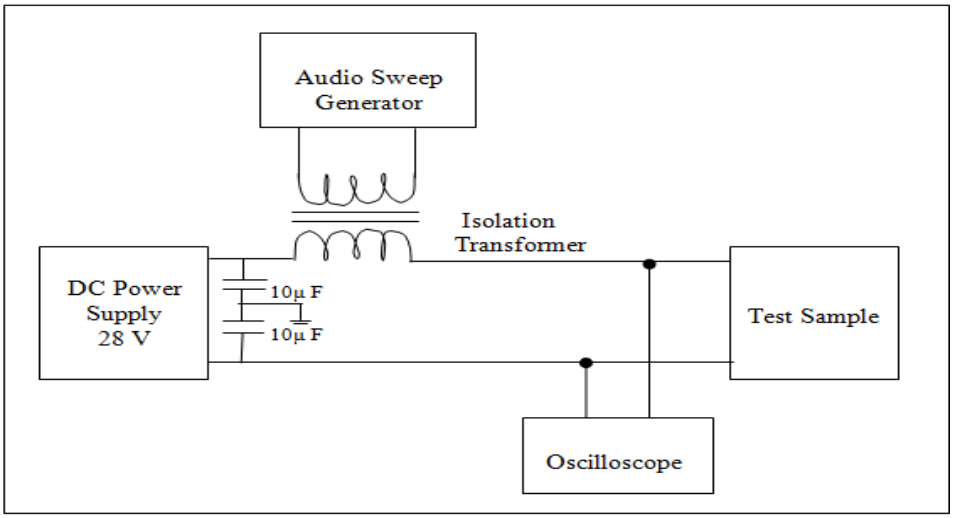

Figure 3.19: CS01 test of MIL STD 461C

The CS01 test indicates that up to 1.5 kHz the converter with Kalman filter has given a lesser attenuation. As the injected audio signal at the output of the converter comes within the band 4.5 V to 5.5 V, the audio frequency will be processed by the Kalman filter. Above 1.5 kHz the output filter attenuates the output signal before giving it to the Kalman filter. So in the band 1.5 kHz - 50 kHz the performance was similar to the one without Kalman filter. The audio rejection up to 1.5 kHz can be taken care by using input voltage feed forward techniques. The CS01 test results are shown in Figure 3.20.

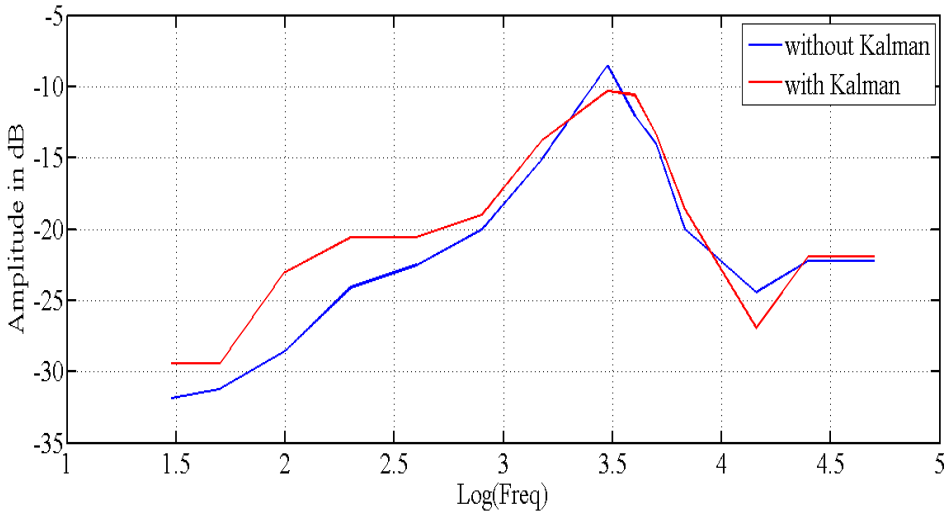

Figure 3.20: CS01 test results

3.6 Conclusion

A reduced state Kalman filter to reduce the limit cycle caused by low resolution ADC in a digitally controlled DC-DC Converter is presented. The limit cycle amplitude reduction is achieved by a reduced state Kalman filter and it was implemented with reduced hardware without affecting the stability margins. The simulation and experimental results show that the proposed scheme had reduced the limit cycle oscillation completely for different resolutions of ADC in a more computationally efficient approach. It was also proved experimentally that the Kalman gain computed offline was effective for all input voltage and load variations.

CHAPTER 4

Reduction in limit cycle oscillation due to low resolution DPWM by switching frequency adjustment

A high resolution DPWM is required for the practical implementation of digitally controlled DC-DC converter. A high resolution DPWM is required to achieve tight output regulation and to avoid undesirable quantization effects such as limit cycle oscillation. This work aims at the usage of low resolution DPWM in digitally controlled DC-DC converter without limit cycle oscillation. The two software methods to improve the effective resolution of DPWM are dithering [3] and sigma delta modulation scheme [14-16]. The details of both the schemes are presented in Chapter 2. In sigma delta modulation scheme as explained earlier the quantization error due to low resolution DPWM is accumulated and when it is equal to one LSB, the duty cycle is adjusted by changing the ON time. The duty ratio thus varied over several switching cycles will have an average value due to the output filter of the converter. This averaging effect increases the effective resolution of the DPWM. But no significant attempts were made to improve the conducted emissions from the converter, apart from improving the effective resolution. In this work, efforts are made to improve the conducted emission also. Conventional PWM converters exhibit high conducted emissions at the fundamental switching frequency and its harmonics. It is well known that conducted emission noise of the converter can be improved by the modulation of the switching frequency. The general tendency of the Frequency Modulation (FM) [51] is to lower the harmonic peaks even though it results in more sidebands spaced by the modulating frequency. Moreover, it is proved that by introducing randomness in switching frequency generation [53], the harmonic power can significantly come down compared to FM and conventional PWM.

This chapter presents a method for the reduction in limit cycle oscillation due to low resolution DPWM by combining the advantages of sigma delta modulation scheme and frequency modulation of switching frequency. In this work, the correction of quantization error due to low resolution DPWM is accomplished

by changing the switching frequency. The error due to the quantization of DPWM was accumulated for few clock cycles and the switching frequency was adjusted in the last cycle such that the duty ratio changes by the number of LSBs corresponding to the quantization error. The quantization error correction increases the effective resolution of DPWM thereby reducing the ripple due to limit cycle oscillations. Further, it also reduces the conducted electromagnetic emissions.

This chapter is organized as follows. The block diagram of a digitally controlled DC-DC buck converter with quantization error correction is described in Section 4.1. The simulation results for a buck converter are given in Section 4.2. The experimental results obtained with a prototype utilizing the quantization error correction are given in Section 4.3. The comparison of the proposed scheme with the existing modulation schemes are also given in Section 4.3. Section 4.4 gives the conclusion.

4.1 Proposed digitally controlled DC-DC converter with quantization error correction

A digitally controlled buck converter with quantization error correction is shown in Figure 4.1. In a conventional digitally controlled DC-DC converter, the output voltage is scaled down, sampled and digitized using ADC. The error is computed by taking the difference between the output of ADC and reference voltage. The error thus computed is fed to a discrete time compensator which computes the digital duty cycle command, $d(n)$. The pre quantized duty cycle $d(n)$ is given to the DPWM that outputs the gate drive pulses at the desired switching frequency based on the digital duty cycle command. Due to the quantization effect of DPWM the duty cycle, $d(n)$ is further quantized to give $d_1(n)$. In the proposed scheme the effective resolution of the DPWM is improved by quantization error correction which is highlighted by the dotted portion in the figure. The error due to the quantization of DPWM is accumulated for consecutive n cycles, and the switching frequency is adjusted in the n^{th} cycle such that the duty ratio changes by the number of LSBs corresponding to the accumulated error.

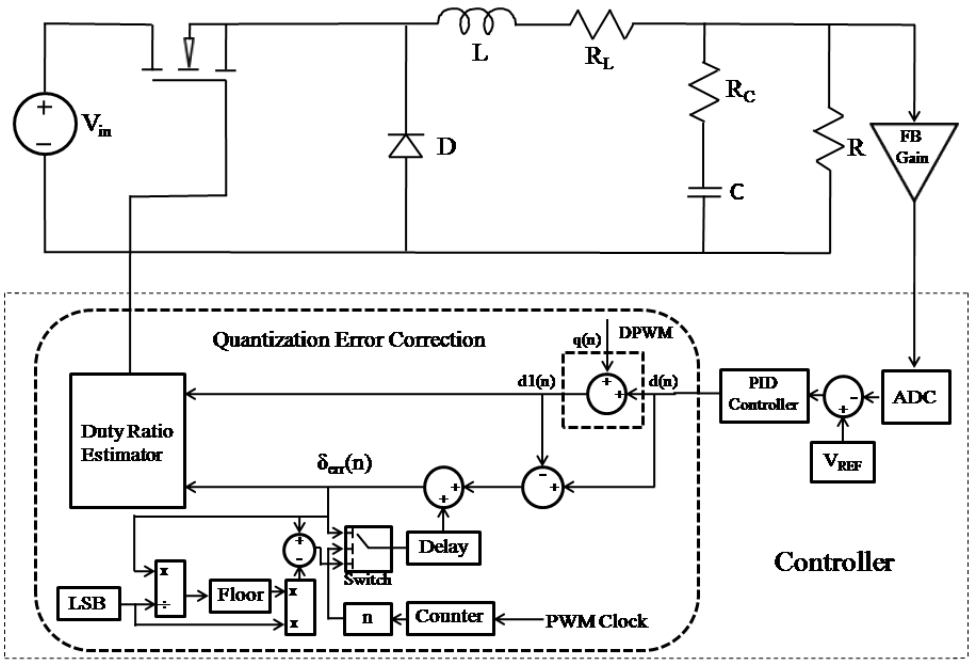

Figure 4.1: Proposed digitally controlled DC-DC converter with quantization error correction

The quantization effect due to the limited resolution of DPWM can be modeled as a noise $q(m)$ added to the non-quantized value $d(m)$ to produce the quantized result, $d_1(m)$.

$$d_1(m) = d(m) + q(m) \tag{4.1}$$

In any conventional digitally controlled DC-DC converter, due to the averaging effect of the LC filter at the output of the converter, the average duty cycle is given by

$$d_{avg} = \frac{\sum_{m=1}^{m=n} d_1(m)}{n} \tag{4.2}$$

Under steady state $d_1(1) = d_1(2) = d_1(n)$ and equation (4.2) becomes

$$d_{avg} = d_1(1) \tag{4.3}$$

In the proposed scheme, the difference between the input of DPWM and the output is accumulated for n clock cycles. The accumulated error is given by

$$\delta_{err}(n) = \sum_{m=1}^{m=n} \langle d(m) - d1(m) \rangle \tag{4.4}$$

And in the n^{th} cycle, the duty cycle is corrected corresponding to the accumulated error. The duty cycle in the n^{th} cycle due to quantization error correction is given by

$$d_1 new(n) = d_1(n) + \delta_{err}(n) \tag{4.5}$$

where $d_1(n)$ is the duty cycle in the n^{th} cycle without any quantization error correction.

Thus with quantization error correction, the average duty cycle averaged up to n cycles can be written as

$$d_{avg} = \frac{(\sum_{m=1}^{m=n-1} d_1(m))) + d_1(n) + \delta_{err}(n)}{n} \tag{4.6}$$

Under steady state, equation (4.6) becomes

$$d_{avg} = \frac{n * d_1(1) + \delta_{err}(n)}{n} \tag{4.7}$$

Therefore, the average value of the duty cycle becomes

$$d_{avg} = d_1(1) + \frac{\delta_{err}(n)}{n} \tag{4.8}$$

Thus from equation (4.8) it is clear that the effective resolution of the DPWM can be improved by quantization error correction. Let us assume that the quantization error changes by one LSB in n cycles then the average duty cycle is

$$d_{avg} = d_1(1) + \frac{LSB}{n} \tag{4.9}$$

In this case, as given in [3], the effective resolution has increased by M bits where $2^M = n$. An increase in the effective resolution of the DPWM brings significant reduction in ripple caused by limit cycle oscillation.

In the proposed scheme, the switching frequency of the converter is changed in the n^{th} cycle to correct the quantization error. Let f_{sw} be the switching frequency of the DC-DC converter. Then the switching frequency in the n^{th} cycle is given by

$$f(new) = \frac{t_{on}(new) * f_{sw}}{t_{on}(old)} \tag{4.10}$$

$t_{on}(old)$ corresponds to the on time for the duty ratio $d_1 new(n)$ for the switching frequency fsw. The $t_{on}(new)$ corresponds to the on time for the duty ratio $d_1 new(n)$ for the switching frequency f(new). The scheme brings reduction in conducted emission levels as the switching frequency is changed in every n^{th} cycle. Again let us assume that the quantization error changes by one LSB in the n^{th} cycle. If the converter is operating at a duty cycle $d_1(n)$ of 30 % at the switching frequency of 400 kHz then the switching frequency changes to 405.2 kHz in the n^{th} cycle to correct the quantization error. Thus the peak power of the conducted emission level at the fundamental frequency fsw will be reduced as the switching frequency is changed in the n^{th} cycle. Also, the switching frequency harmonics will be reduced. Since the implementation is done in the digital domain the following equations were implemented in the controller for error correction.

The duty ratio is given by

$$d_{digital} = t_{ondigital}/T_{digital} \tag{4.11}$$

$t_{ondigital}$ is the digital word equivalent of the on time of the PWM signal.$T_{digital}$ is the digital word equivalent of the period of the PWM signal. To compute the switching frequency at the n^{th} cycle, as the implementation is in the digital domain, the count value is computed based on how many LSBs the accumulated error value will correspond to in the n^{th} cycle and is given by

$$count = Floor\left\lfloor\frac{\delta_{err}(n)}{LSB}\right\rfloor \tag{4.12}$$

The duty ratio in the n^{th} cycle that correct the quantization error is given by

$$d_{digital}(n) = \frac{t_{ondigital} + count}{T_{digital}} \tag{4.13}$$

In this scheme as in sigma delta modulation scheme the on time is not adjusted to change the duty ratio. Instead of that the switching frequency is adjusted based on the equation given below.

$$\frac{t_{ondigital} + count}{T_{digital}} = \frac{t_{ondigital}}{T1_{digital}} \tag{4.14}$$

$T1_{digital}$ is the period corresponding to the new switching frequency. Since the accumulated error, $\delta_{err}(n)$ will not be an integer multiple of LSB, in the subsequent cycle, the difference between the accumulated value of error and the count value times the LSB is given to the accumulator as the residual value. That is

$$\delta_{residual}(n) = \delta_{err}(n) - count * LSB \tag{4.15}$$

A brief description of sigma delta modulation and the relationship between the proposed method and sigma delta modulation is presented in Appendix 3. The number of clock cycles, n, for which the quantization error is accumulated is decided by the corner frequency of the output filter. Averaging for n clock cycles will result in an additional ac ripple with frequency of f_{sw}/n [3]. It is desirable that the output filter should provide sufficient attenuation at f_{sw}/n. In the present design, the corner frequency of the output filter is 5 kHz. If averaging is done for three clock cycles, an additional content at 133 kHz will be superimposed on the ac ripple if the switching frequency is 400 kHz. In this case, the output filter will provide an attenuation of more than 80 dB. Experimentally it is verified that the scheme gives significant results if averaging is done for three cycles. A ripple rejection of 17 dB could be achieved by accumulating the error for consecutive three cycles and adjusting the error in the third cycle. The implementation of equation (4.12) to equation (4.15) in the digital domain is shown in Figure 4.1. Here, even though the effective improvement in resolution is less compared to that of sigma delta modulation, it reduces the conducted emission levels considerably.

4.2 Simulation results

The Simulink model of the digitally controlled buck DC DC converter used for simulation is shown in Figure 4.2.

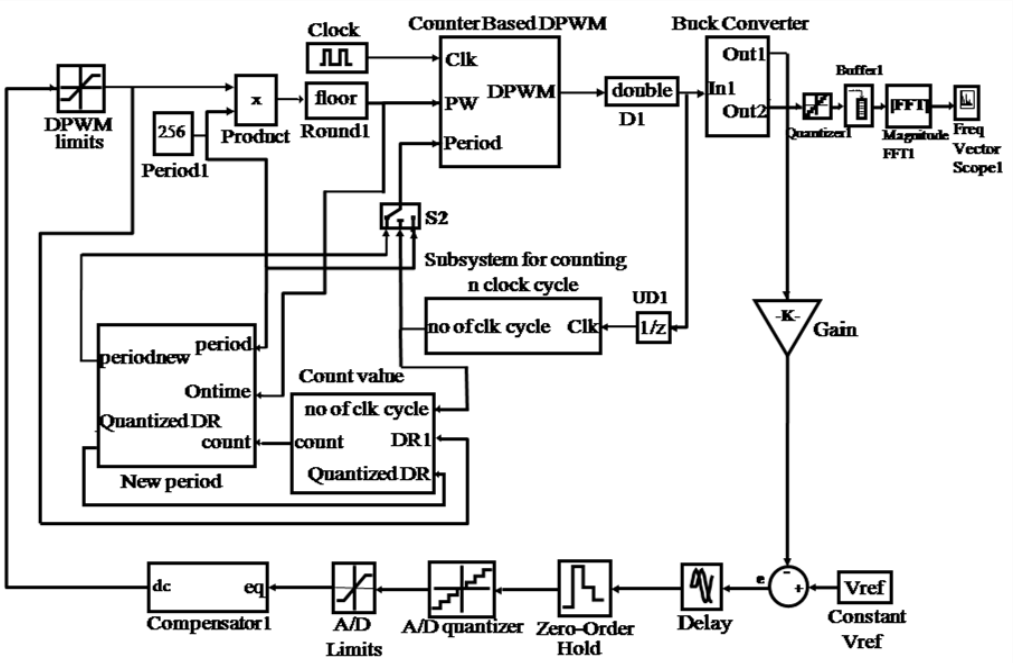

Figure 4.2: Simulink model of the digitally controlled DC-DC Converter with quantization error correction

The main subsystems of the Simulink model are the 'buck converter' that models the power stage of the buck topology, 'number of clock cycle' that counts the PWM clock cycle, 'count' that computes the count value based on equation (4.12), ' New period' that computes the new period based on equation (4.14) and the 'Counter Based DPWM'.

The buck converter parameters are $L = 100\mu H, C = 22\mu F,$
Output voltage $Vout = 5\ V,$ Input voltage $Vin = 12 - 18\ V,$
Switching frequency $fsw = 400\ kHZ,$ ESR of capacitor $Rc = 0.1\ \Omega,$
load resistanc $R = 2.5\ \Omega,$ series resistance of inductor $RL = 0.025\ \Omega.$

The DPWM is initially configured for 8 bits and the ADC is configured for 10-bit resolution. The sampling period is equal to the period of switching frequency, $T_S = 2.5\ \mu s$. The discrete-time transfer function $G_{OL}(z)$ of the overall open loop system, which takes into account the power stage, zero order hold, the feedback gain comprising of ADC gain, feedback factor and DPWM gain, the total computational delay in the control loop, that follows from the modeling approach described in [20] [22] [23], can be expressed as

$$G_{0L}(z) = \frac{0.02309z - 0.006403}{z^2 - 1.952z + 0.9543} \tag{4.16}$$

In this model the computational delay is taken as $0.5\ T_S$.

A suitable controller $G_C(z)$ is designed as given in [23] to compensate the above system $G_{OL}(z)$ in such a way that gain rolls off at a slope of –20 dB/decade at 0 dB and provides sufficient margin so as to ensure stability. The discrete PID controller is designed and is given by

$$G_C(z) = \frac{U}{E} = \frac{22.6(z - 0.966)(z - 0.991)}{z(z - 1)} \tag{4.17}$$

where U is the control output and E is the error voltage. The compensator provides a phase margin more than 45°and bandwidth of 25 kHz. The simulated open loop response of the converter with controller is given in Figure 4.3.

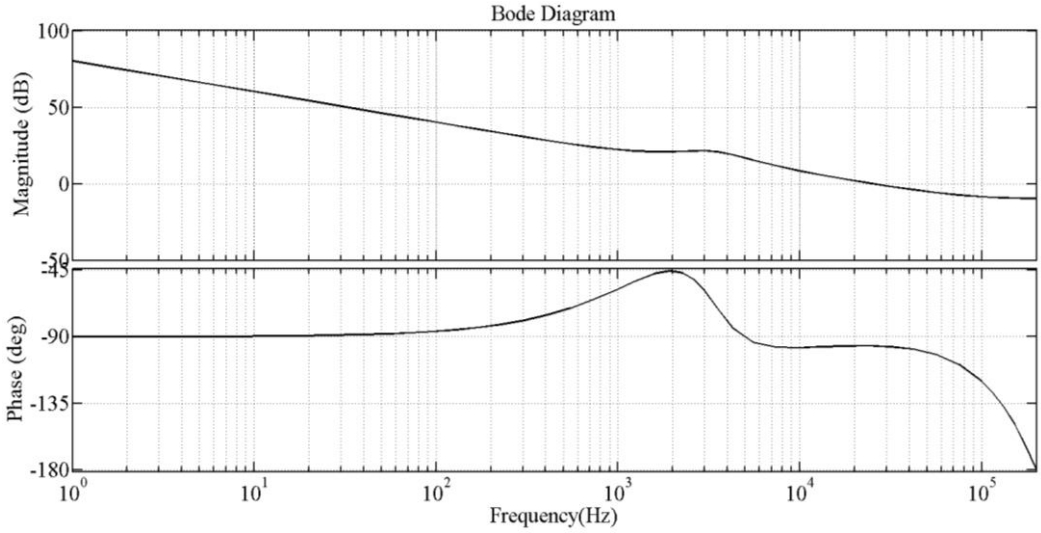

Figure 4.3: Open loop response of the converter (converter and compensator)

The limit cycle oscillation without the Quantization Error Correction (QEC) is shown in Figure.4.4. Here the ripple is 30 mV and the ripple frequency is 5 kHz which clearly indicates limit cycle oscillation due to low resolution DPWM. Figure 4.5 shows that the ripple at the output of the converter with quantization error correction. Quantization error correction as proposed in this work has reduced the limit cycle oscillation. The proposed scheme has brought a significant reduction in ripple amplitude. The ripple is 20 mV and the frequency is the switching

frequency which indicates the reduction of limit cycle oscillation. To obtain the conducted emissions from the converter, the spectrum of the input ripple current was taken. Simulation results of the conducted emissions from the input line, without and with quantization error correction are shown in Figures 4.6 and Figure 4.7 respectively. A reduction of 25 dB in the conducted emission level of the fundamental switching frequency components is clearly seen.

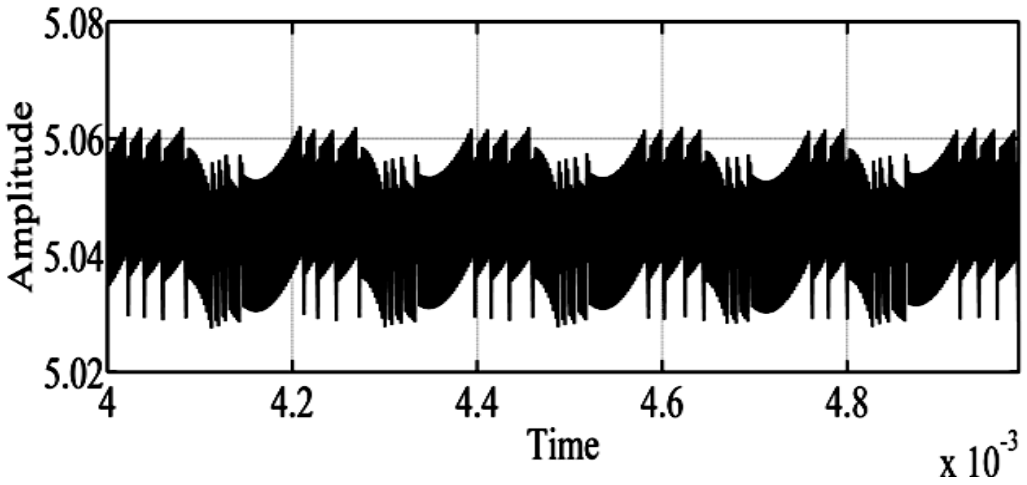

Figure 4.4: Simulation results showing the ripple at the output of the converter without QEC

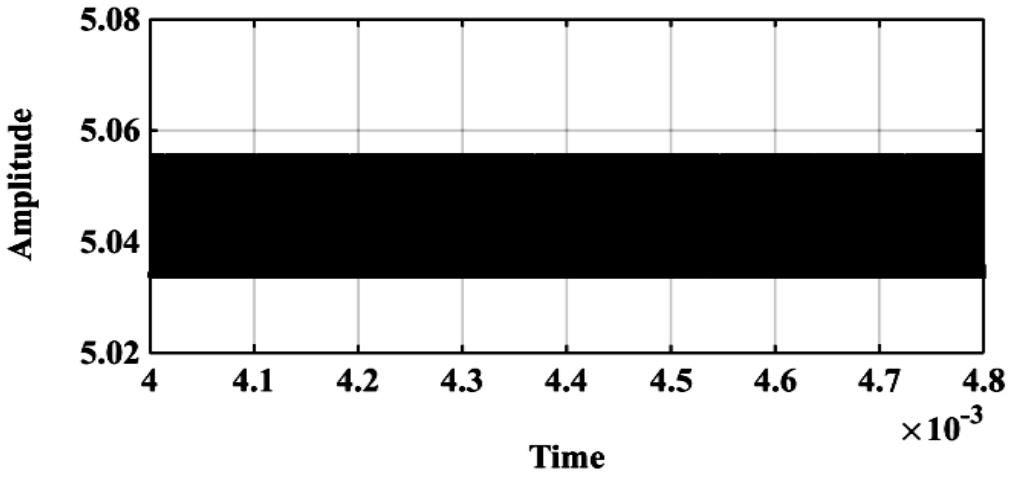

Figure 4.5: Simulation results showing the ripple at the output of the converter with QEC

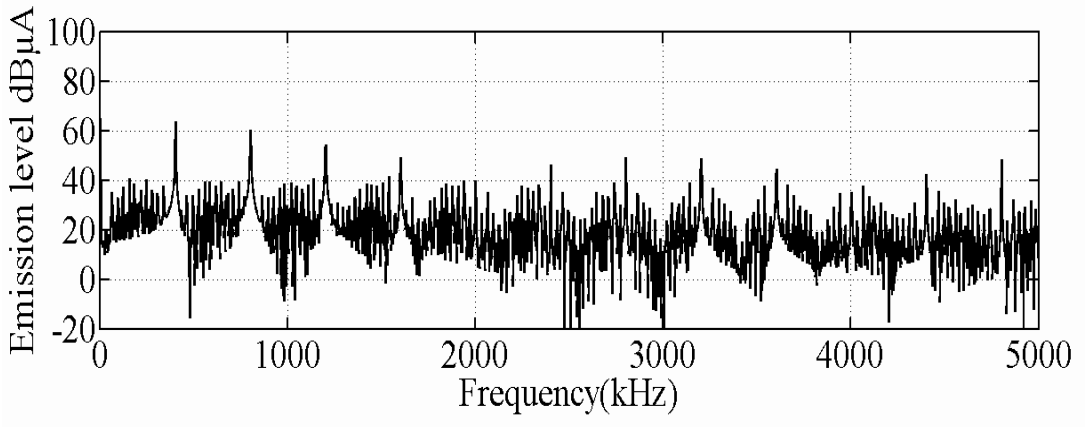

Figure 4.6: Simulation results showing emission level without QEC

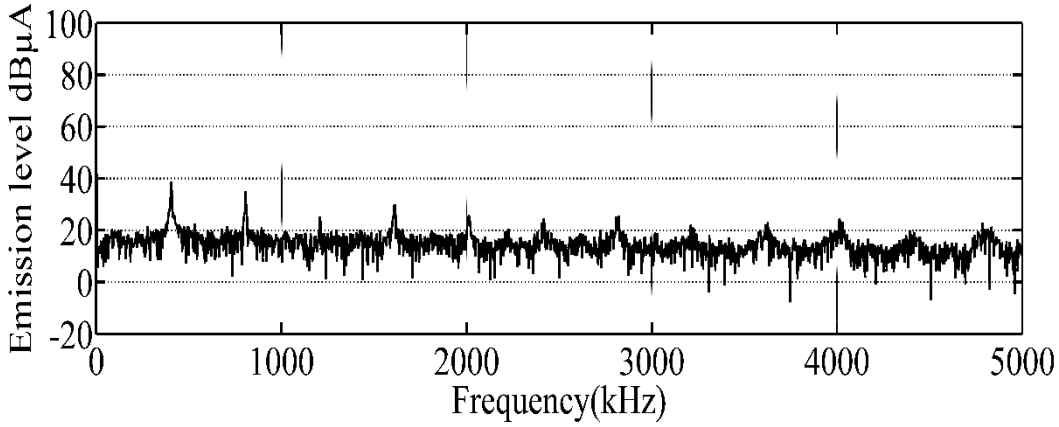

Figure 4.7: Simulation results showing emission level with QEC

4.3 Experimental results

The prototype model of the digitally controlled buck converter was implemented using dsPIC33FJ16GS502, a 16-bit digital signal controller, from Microchip Technology Inc. The DPWM was configured for 8 bit and the ADC was configured for 10-bit resolution with analog input range of 0 to 3.3V. The output filter circuit was the same as that used in the simulations. Pre calculated PID coefficients were stored in Q12 format of fixed point representation. The switching frequency and sampling rate were fixed as 400 kHz. The output of the converter without quantization error correction is illustrated in Figure 4.8. The ripple voltage was found to be around 290 mV with ripple frequency of 5 kHz which indicates limit cycle oscillation. The ripple is more compared to the simulation results. In the

simulation, the round off errors, finite word length of the DSP processor, scaling of the inputs, outputs and PID coefficients due to the limited dynamic range of the fixed point implementation, has not been modeled. Detailed mathematical analysis on the truncation error due to the usage of fixed point processor has been presented [64]. It has been proved that the truncation errors greatly affect the DC gain and the effect for Q12 format of fixed point representation of PID coefficients has also been presented [64]. Figure 4.9 shows the output of the converter with quantization error correction by using the proposed scheme. The proposed scheme reduces the ripple from 290 mV to 40 mV.

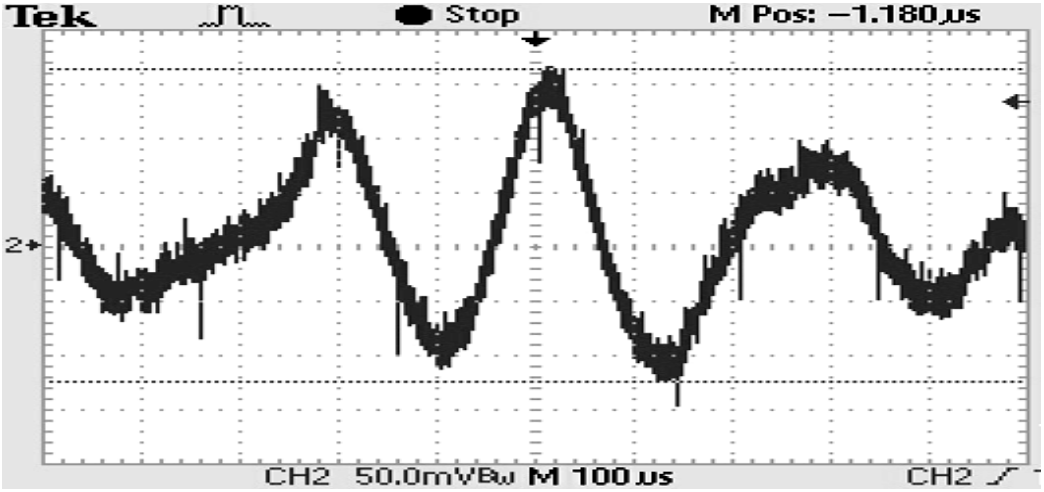

Figure 4.8: Ripple at the output of converter (without QEC) Y axis scale : 50 mV, X axis scale : 100 µsec

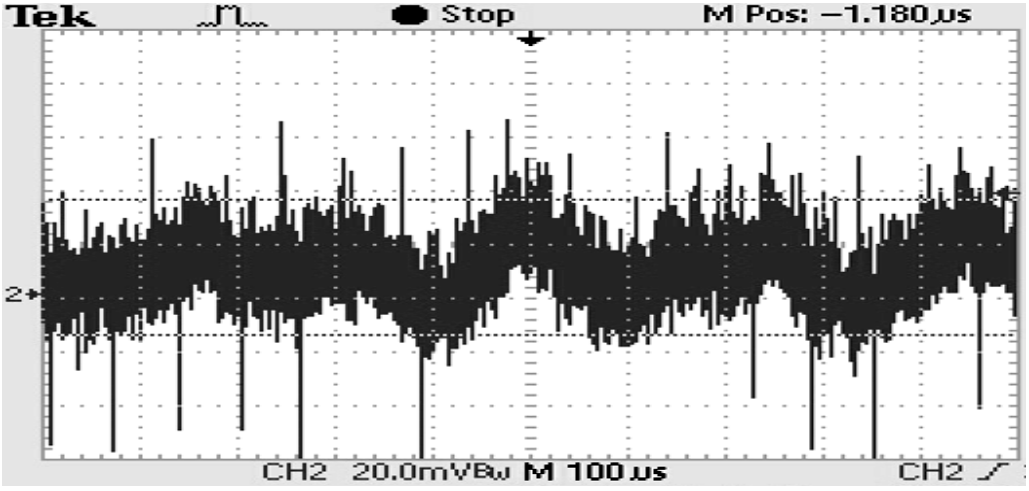

Figure 4.9: Ripple at the output of converter (with QEC) Y axis scale:20 mV, X axis scale:100 µsec

The proposed scheme brings reduction only in the ripple due to limit cycle oscillation which is caused by low resolution DPWM. Hence the amplitude of the spike in both the plots show around 100 mV and only the low frequency components amplitude has come down.

The transient response of the converter is taken to study the effect of introduction of QEC on the stability margins. It is found that there is no considerable variation in the transient response which confirms that the stability margins are not affected by introduction of QEC. Figure 3.18a and Figure 3.18b shows the transient response of the converter, without QEC and with QEC respectively when the load changes from 50 to 100 % of the maximum load. The output of the converter (5 V) is captured in the AC coupling mode of the oscilloscope. From Figure 4.10a and Figure 4.10b, it is noted that the overshoot is less than 17%, which indicates that the phase margin is more than 45º.

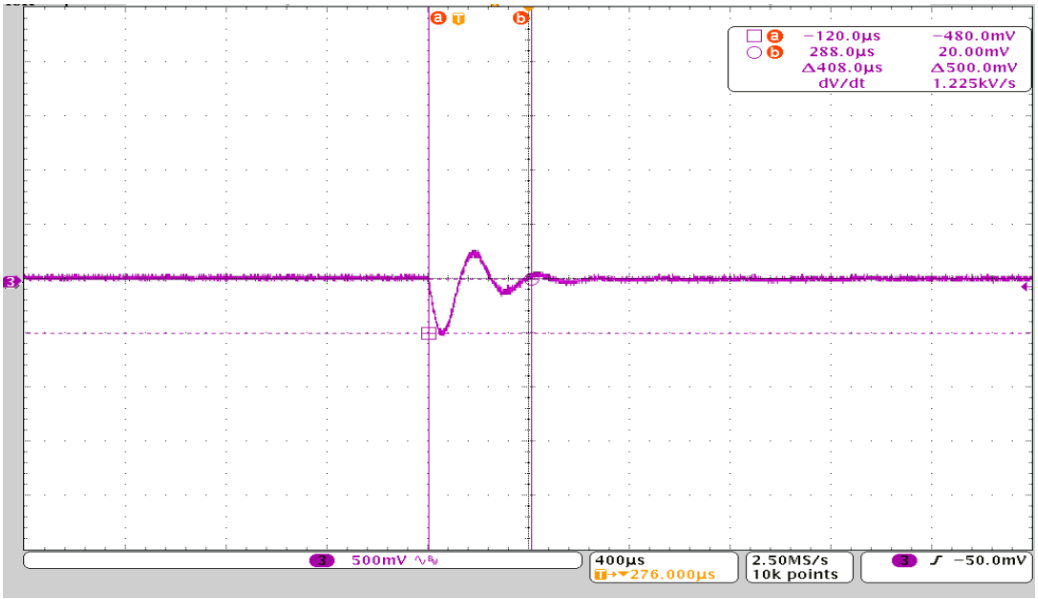

Figure 4.10a

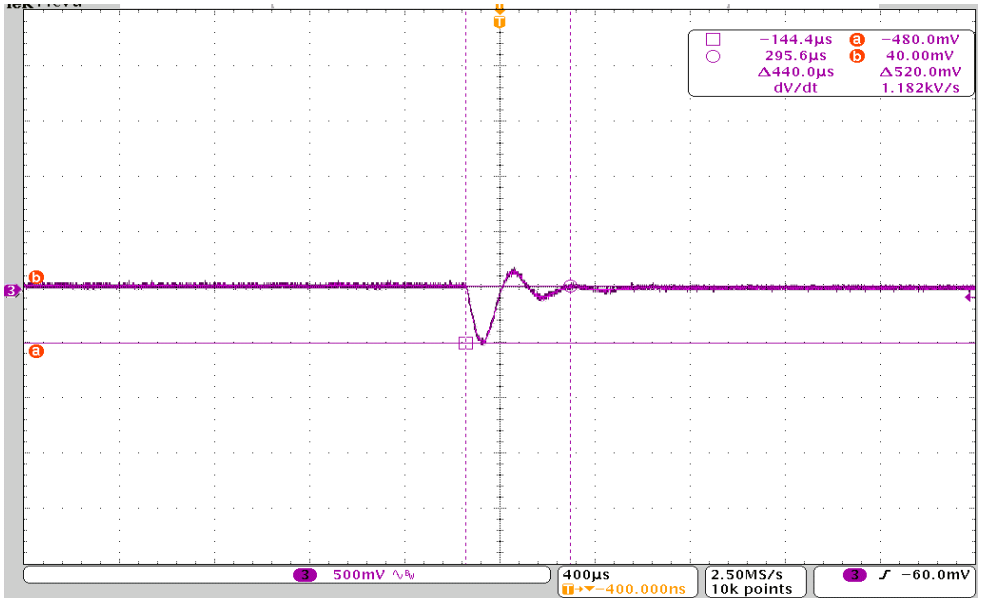

Figure 4.10b

Figure 4.10: Transient response of the converter (AC coupling mode of oscilloscope) without QEC (4.10a) and with QEC (4.10 b)

To study the effect of the change in switching frequency, the spectrum of the input current was measured using the test set up of the conducted emission test, CE03 of MIL STD 461C. The CE03 test of MIL STD 461C is given in Appendix 4. The input current was measured using the current probe of M/S Ailtech NM 17/27, Model No 91650-1B and the EMI Receiver used was of M/S Rohde and Schwarz make, ESU 20 Hz - 26.5 GHz. A linear scan of 15 kHz - 50 MHz was used with sweep time of 1second and IF bandwidth of 1 kHz for getting fine resolution. Figure 4.11 shows the conducted emission for the converter without QEC. Figure 4.12 shows the conducted emission for the converter with the proposed QEC scheme. The plots clearly indicate that there is a reduction in the peaks across the entire frequency span of measurement. The emission level at 400 kHz is 65 dBµA without quantization error correction. Significant reduction in the fundamental component from 65 dBµA to 40 dBµA could be achieved by changing the switching frequency for quantization error correction.

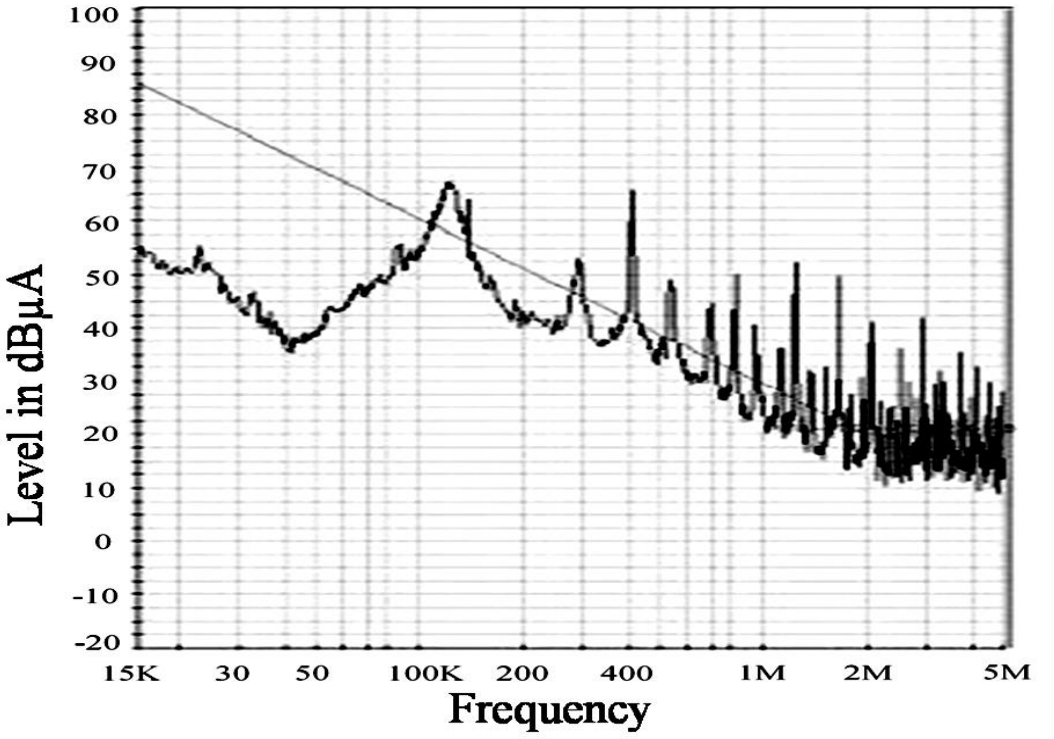

Figure 4.11: Conducted emission level without QEC (CE03 test of MIL STD 461C)

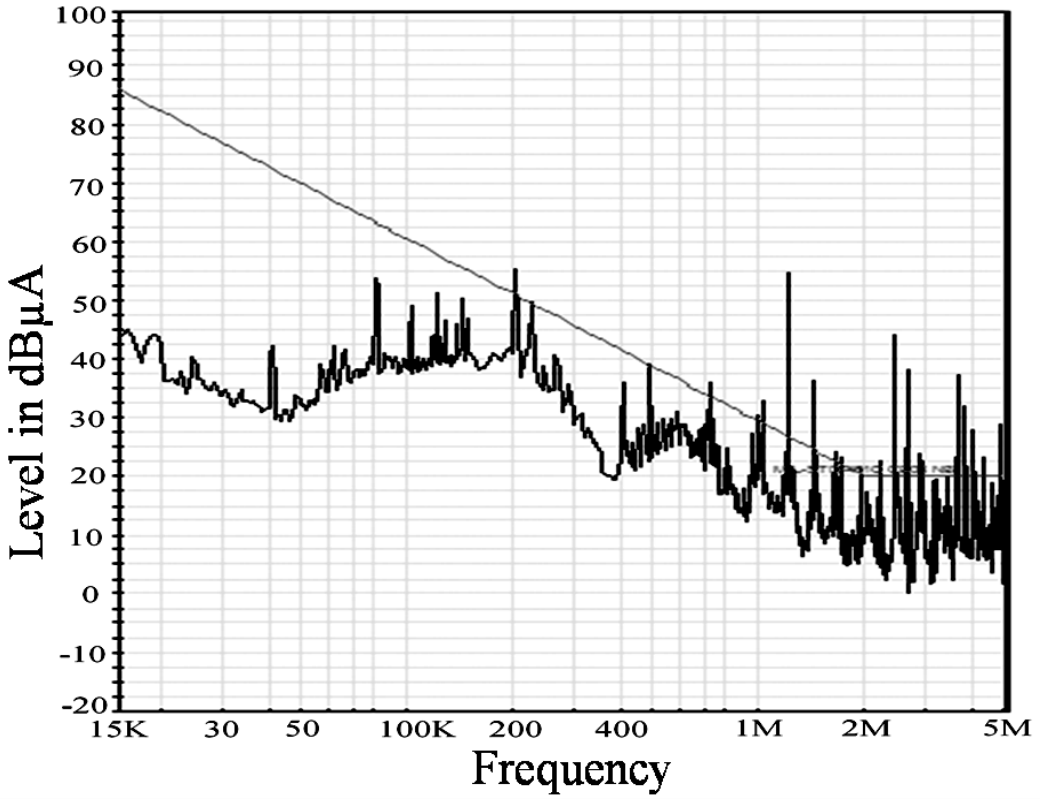

Figure 4.12: CE03 plot with QEC

Thus quantization error correction by changing the switching frequency brings a reduction of 17 dB in the output noise due to the limit cycle oscillation and a reduction of 25 dB in the fundamental component of the switching frequency in the conducted emission levels.

Comparison of the different modulation schemes with the proposed scheme is given in Table 4.1. The frequency modulation, random carrier frequency technique and spread spectrum techniques are some of the different modulation schemes solely aimed at reducing the conducted emission levels. The sigma delta modulation method is a method used to improve the effective resolution of the DPWM. This scheme has the same conducted emission level as that of the standard PWM scheme. The proposed scheme combines the advantages of both the sigma delta Modulation Scheme and random carrier frequency technique.

Table 4.1: Comparison of different modulation schemes

Modulation Scheme	Reduction in conducted emission compared to standard PWM scheme	Reduction in limit cycle oscillation
Frequency Modulation [52]	10 dB reduction in the whole band of conducted EMI	No
Spread spectrum technique [54]	23.4 dB reduction in the conducted EMI peak (fundamental)	No
Sigma delta modulation [14][15]	Same as Standard PWM scheme	Reduction of limit cycle oscillation
Proposed scheme	25 dB reduction in the conducted EMI peak (fundamental)	17 dB reduction in ripple

4.4 Conclusion

This chapter introduces a scheme that combines the advantages of frequency modulation of switching frequency and the sigma delta modulation scheme used to improve the effective resolution of DPWM. In the proposed scheme the switching frequency is adjusted in the n^{th} cycle such that the duty ratio changes by the number of LSBs corresponding to the quantization error accumulated up to the n^{th} cycle.

The change of switching frequency in the n^{th} cycle, for quantization error correction, brings reduction in the ripple due to limit cycle oscillations and in conducted emissions levels. Reduction in ripple of around 17 dB and reduction in conducted emission level of 25 dB has been achieved. This scheme has significant advantage over sigma delta DPWMs as the conducted emission levels have also been drastically reduced in addition to the improvement in the effective resolution.

CHAPTER 5

A proposed configuration for a high frequency digitally controlled DC-DC converter with low resolution ADC and DPWM

This chapter focuses on arriving at a most appropriate configuration for a high frequency controlled DC-DC converter with respect to the resolution of ADC and DPWM. In this chapter the advantages of the schemes mentioned in Chapters 3 & 4 are combined. The reduced state Kalman filter for giving the optimum estimate of the output voltage based on the noisy measurement from low resolution ADC and the quantization error correction due to low resolution DPWM by switching frequency adjustment are combined. Thus by using these two schemes, a low resolution ADC with 6-bit resolution and 7-bit DPWM has been used in a digitally controlled DC-DC converter without any limit cycle oscillation and performance degradation. The simulation results for various resolutions of ADC and DPWM have been presented and a most appropriate configuration is arrived at. The experimental results are also presented.

The chapter is organized as follows. In Section 5.1, the digitally controlled DC-DC converter using the proposed scheme is described. In Section 5.2 simulation results are provided. In Section 5.3 the experimental results with detailed discussion are provided. The conclusion is given in Section 5.4.

5.1 System description

Figure 5.1 shows the block diagram of a digitally controlled PWM DC-DC buck converter that combines the advantages of the reduced state Kalman filter and the quantization error correction. The resolution of ADC and DPWM are varied and utilizing the advantages of reduced state Kalman filter and the quantization error correction, an attempt to arrive at the most appropriate configuration is made.

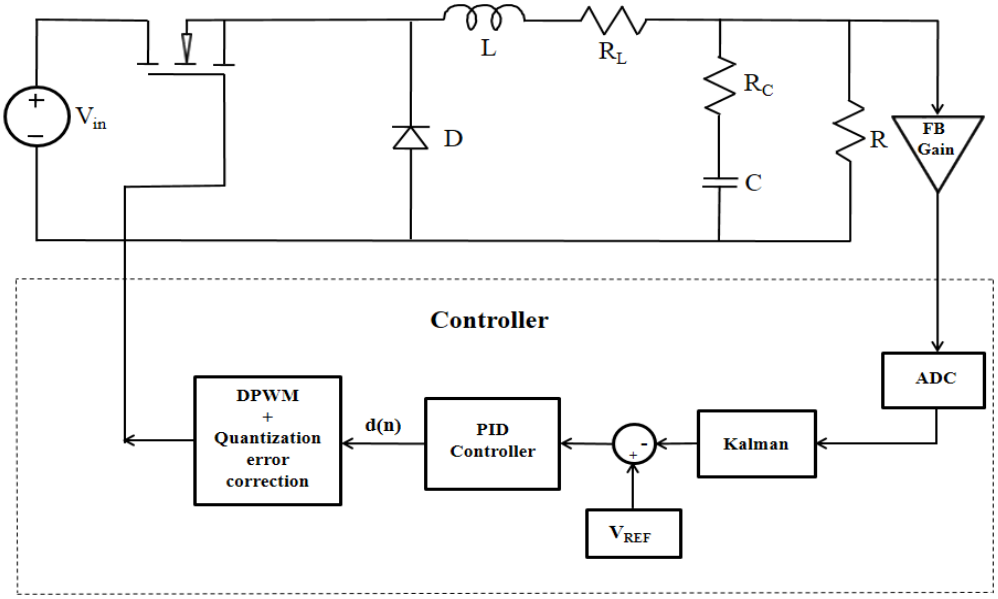

Figure 5.1a: Block diagram of the configuration of digitally controlled DC- DC converter combining reduced state Kalman filter and QEC

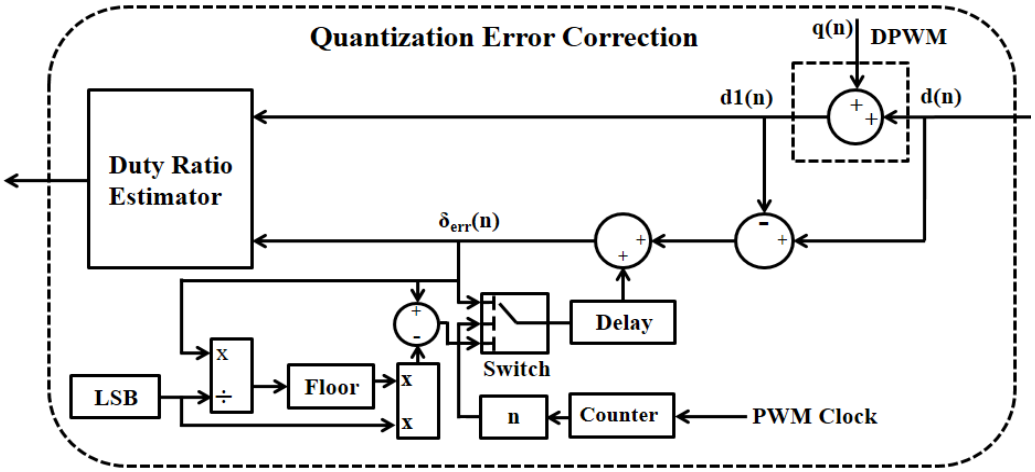

Figure 5.1b: Quantization error correction

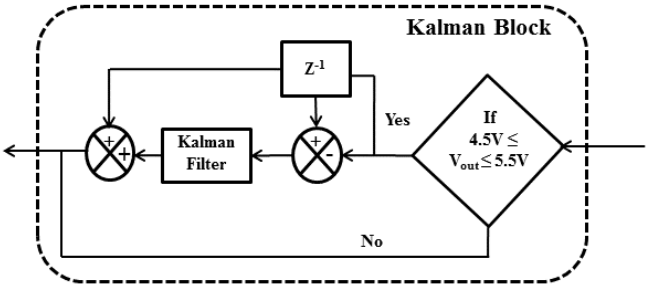

Figure 5.1c: Kalman Filter

5.2 Simulation results

The parameters of the converter and the PID compensator are the same as in chapter 3. The Simulink model used for the simulation combines the model presented in chapter 3 and chapter 4. As mentioned in chapter 3, for low resolution ADC, limit cycle oscillation may occur if the reference voltage does not coincide with zero error bin. Hence all the simulations were carried out with the same reference voltage and the configuration that resulted in limit cycle oscillation was studied to find the effect of the combined scheme. Different resolutions of ADC and DPWM were used for the simulations. Four different cases were simulated. In Case I, low resolution ADC and DPWM without Kalman filter and QEC was simulated. In Case II, Kalman filter was alone simulated and in case III, QEC alone was simulated. In case 1V, both Kalman and QEC was applied to low resolution ADC and DPWM. The Kalman filter reduces but does not completely eliminate the limit cycle oscillation due to low resolution ADC and DPWM. Similarly, quantization error correction alone will reduce the limit cycle oscillation to a great extent but this also cannot completely eliminate the limit cycle oscillation. Whereas Kalman filter and quantization error correction (QEC) together can completely reduce limit cycle oscillation. Even with low resolution ADC and DPWM, limit cycle oscillation has been reduced by combining the schemes.

The simulation was first carried out for 10-bit ADC and 11-bit DPWM to evaluate the PID coefficients of the converter. The output voltage is 4.93V with load regulation of 0.3 % and line regulation of 0.01 %. The ripple is less than 20 mV at 400 kHz. The simulation was carried out for 6-bit ADC and 7-bit DPWM for a high frequency digitally controlled DC- DC converter. The input voltage is set at 18 V and the load current is at 500 mA. The reference voltage is kept at 1.596 V for all the simulations given below. The simulation results shown in Figure 5.2 gives the output from the converter for the four different cases. 1) Without any Kalman filter and QEC 2) Kalman filter alone 3) QEC alone and 4) Reduced state Kalman filter and QEC. Without the Kalman filter and QEC, the ripple voltage is 60 mV at around 2.5 kHz. The output voltage is 4.9 V. With Kalman filter alone, the ripple

has come down to 10 mV at 45 kHz. The output voltage is 4.975 V. With QEC alone, ripple is 6 mV at 45 kHz with output voltage at 4.875 V. For the case with Kalman filter and QEC, the ripple voltage is 4mV at 400 kHz. The output voltage is at 4.875 V. In the figure the black plot is not clearly visible as it is embedded within the pink plot. This clearly indicates that by combining both the schemes limit cycle oscillation has been reduced drastically.

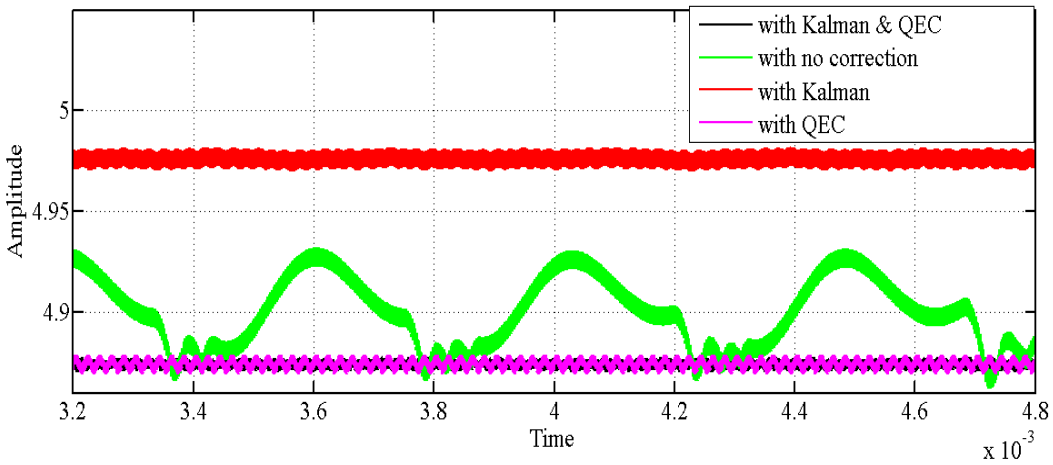

Figure 5.2: Output of converter, 6-bit ADC and 7-bit DPWM, Input voltage 18 V and load current of 500 mA.

To find out the load regulation, the load current is changed to 2 A. Figure 5.3 gives the plot for the four different cases for input voltage of 18 V and load current of 2 A. Without the Kalman filter and QEC, the ripple voltage is 14mV at around 10 kHz. The output voltage is 4.94 V. With Kalman filter alone, the ripple is 10 mV at 45 kHz. The output voltage is 4.876 V. With QEC alone, ripple is 4 mV at 45 kHz with output voltage at 4.874 V. For the case with Kalman filter and QEC, the ripple voltage is 2 mV at 400 kHz. The output voltage is at 4.871 V. The load regulation is 0.1 %. By combining the scheme, the limit cycle oscillation could be drastically reduced without affecting the load regulation. The output set value has changed but the change in set value can be corrected by adjusting the reference voltage. Figure 5.4 shows the expanded view of the output voltage for the combined scheme and it clearly shows that the limit cycle has been drastically reduced.

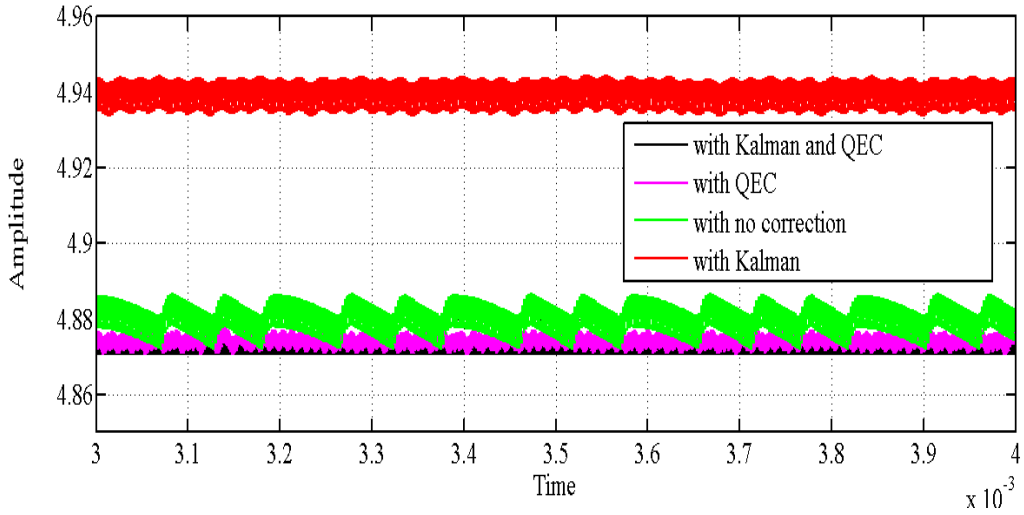

Figure 5.3: Output of converter, 6-bit ADC and 7-bit DPWM, Input voltage 18 V and load current of 2A

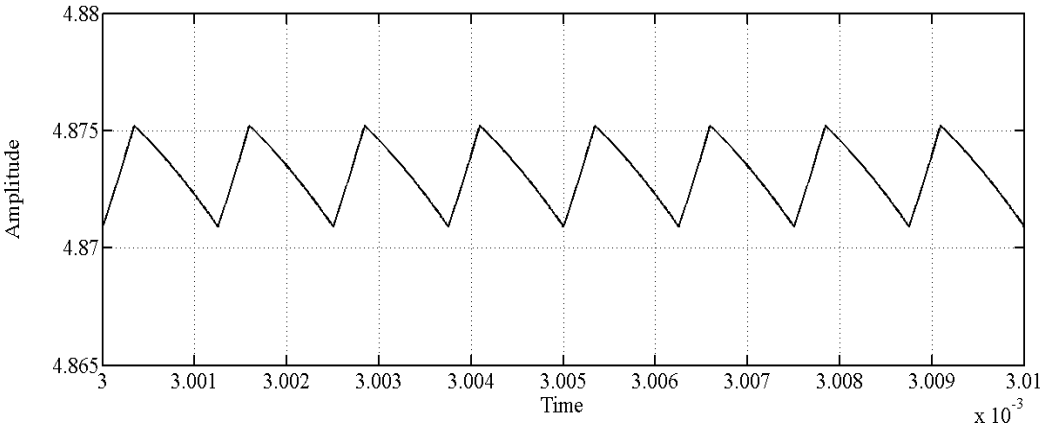

Figure 5.4: Output of converter, 6-bit ADC and 7-bit DPWM, Input voltage 18 V and load current of 2 A with Kalman & QEC (expanded view)

To compute the line regulation, the input voltage is changed to 12 V with the load current at 2.5 A and the output plot is given in Figure 5.5. Without the Kalman filter and QEC, the ripple voltage is 60 mV at around 2.5 kHz. The output voltage is 4.9 V. With Kalman filter alone, the ripple has come down to 10mV at 45 kHz. The output voltage is 4.9475 V. With QEC alone, ripple is 6 mV at 45 kHz with output voltage at 4.875 V. For the case with Kalman filter and QEC, the ripple voltage is 4 mV at 400 kHz. The output voltage is at 4.83 V. By combining the scheme, the limit cycle oscillation could be drastically reduced with line regulation of 0.85 %.

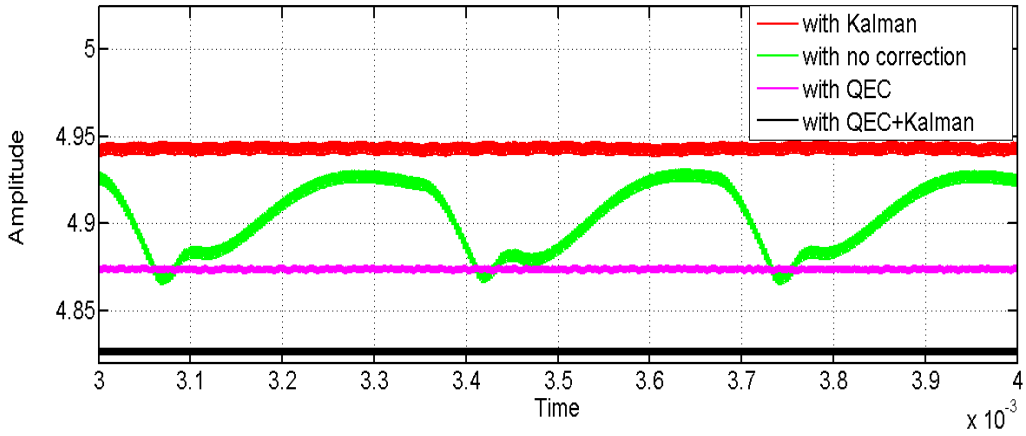

Figure 5.5: Output of converter, 6-bit ADC and 7-bit DPWM, Input voltage 12 V and load current of 2 A

The simulation was repeated for 5-bit ADC and 6-bit DPWM. The result for the input voltage of 12 V and load condition of 500 mA is shown Figure 5.6. The plot shows that with Kalman filter and QEC, the limit cycle oscillation has been reduced significantly.

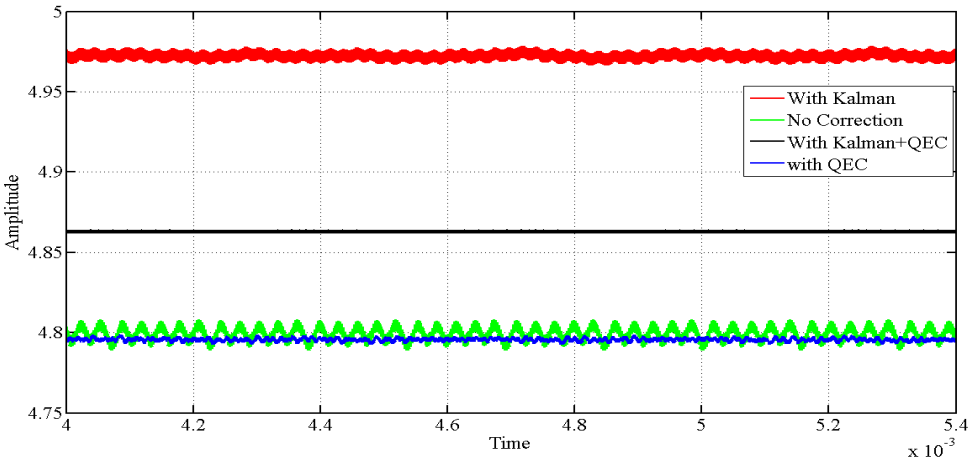

Figure 5.6: Output of converter, 5-bit ADC and 6-bit DPWM, Input voltage 12 V and load current of 500 mA

The simulation was repeated for 8-bit ADC and 9-bit DPWM and the results are shown in Figure 5.7. The amplitude of the limit oscillation was very less (less than 10mV) for this reference voltage and this has been significantly reduced by using Kalman filter and QEC. As given in Appendix 1, the gain of the DPWM and ADC depends on the amplitude of the input signal and the offset of the input signal. For some operating points, ie for some V_{ref}, a low resolution DPWM can result in

operation without limit cycle oscillation [76]. It happens when one of the coarse quantization steps causes the output voltage to fit inside the zero-error bin. In the simulations, the reference voltage is 1.596V. For a 5-bit ADC, the quantization level will result in 1.59677V whereas for 6-bit ADC, the quantization level is 1.571 V or 1.623V. Hence more limit cycle oscillations are seen for 6-bit compared to 5-bit. If the reference voltage is changed, then it can be the other way.

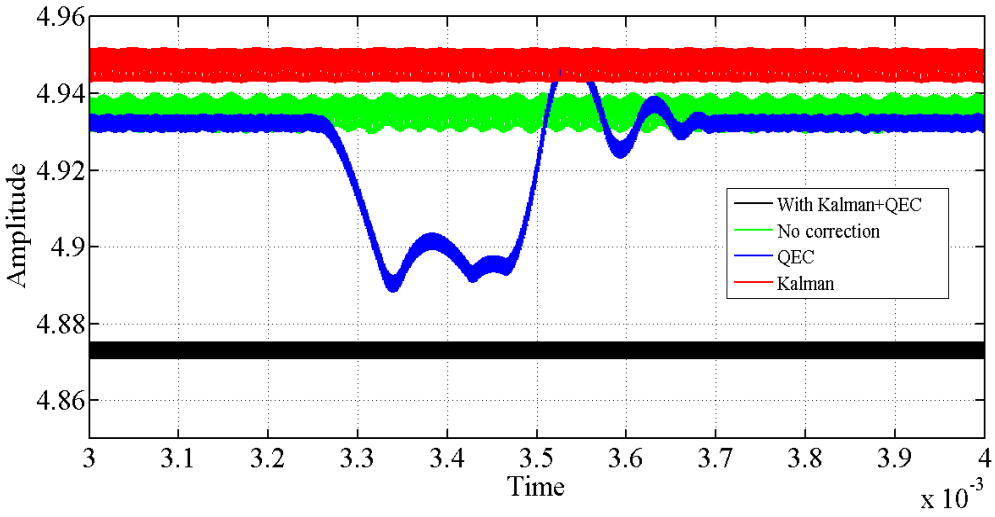

Figure 5.7: Output of converter, 8-bit ADC and 9-bit DPWM, Input voltage 18 V and load current of 2A

The simulation was repeated for 9-bit ADC and 10-bit DPWM. In Figure 5.7, it is clear that the limit cycle oscillation for QEC is more than the case with no correction. When low resolution ADC is used, it is necessary that Kalman filter should be used, in addition to QEC, to reduce the limit cycle oscillation. It is clear from these simulations that only the combined scheme with Kalman filter and quantization error correction reduces limit cycle oscillation significantly.

5.3 Experimental results

The experimental set up was the same as mentioned in Chapter 3. The ADC is configured for 6-bit and the DPWM for 7-bit. In the first case, error correction was not incorporated. The input voltage is 18 V and the load current is 500 mA. The output voltage acquired using an AC coupled oscilloscope is shown in the Figure 5.8a. The limit cycle oscillation is 192 mV at frequency of 3.57 kHz. The

load is changed to 2 A and the plot is shown in Figure 5.8b. The amplitude of limit cycle oscillation is 154 mV at 2.809 kHz. The input voltage is changed to 12 V and the output is given in Figure 5.8c. The amplitude of limit cycle oscillation is 120 mV at 1.894 kHz.

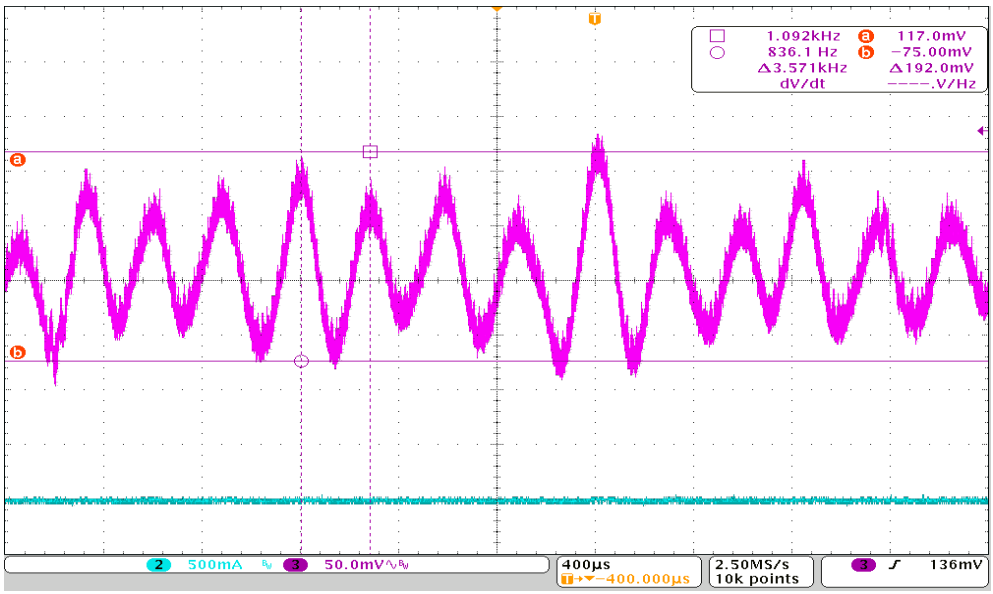

Figure 5.8a: Output of the converter with no error correction (pink trace), Input voltage of 18V and load condition of 500mA. The load current is shown by blue trace

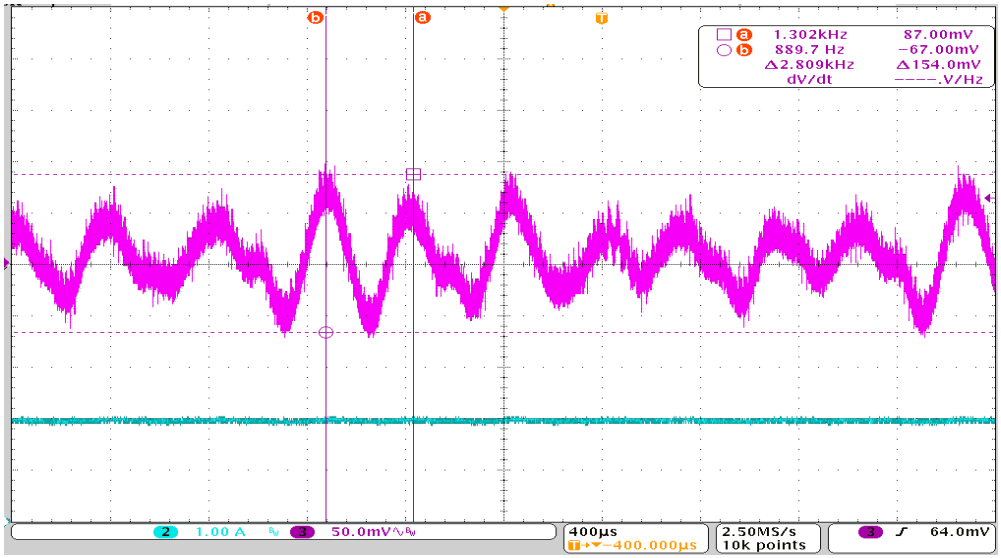

Figure 5.8b: Output of the converter with no error correction (pink trace), Input voltage of 18V and load condition of 2A. The load current is shown by blue trace

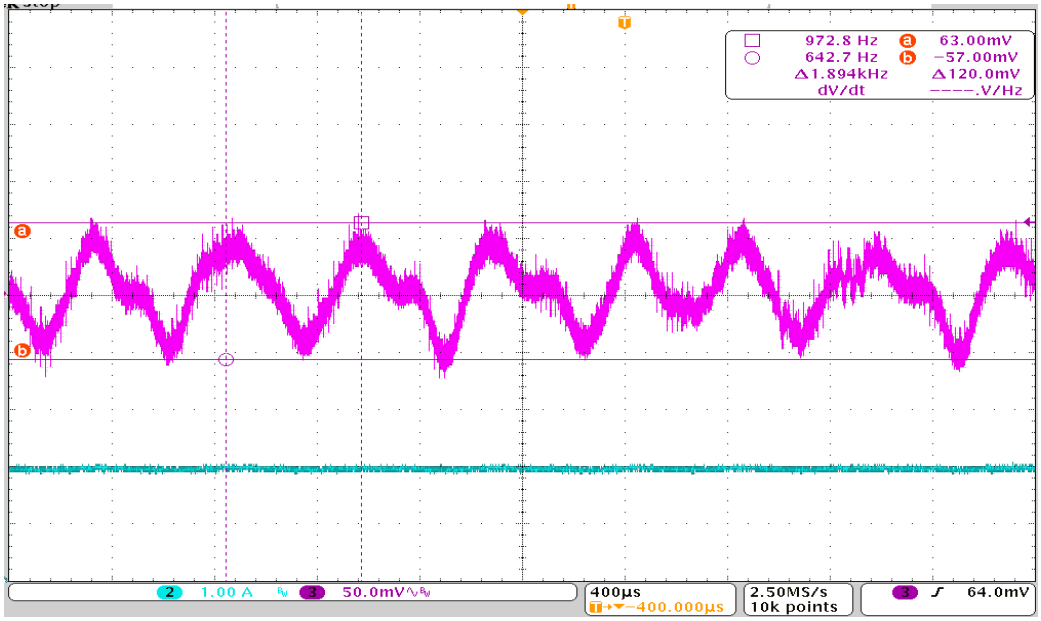

Figure 5.8c: Output of the converter with no error correction (pink trace), Input voltage of 12V and load condition of 2A. The load current is shown by blue trace.

In the second case, only Kalman filter was introduced to give the optimum estimate from the noisy measurement from ADC. The firmware was identical to chapter 3 with only the resolution of DPWM changed to 7-bit. The input voltage is 18V and the load current is 500 mA. The limit cycle oscillation is 43 mV at frequency of 31.25 kHz and the plot is given in Figure 5.9a. The load is changed to 2 A and the plot is shown in Figure 5.9b. The amplitude of limit cycle oscillation is 55 mV at 31.25 kHz. The input voltage is changed to 12 V and the load condition is set at 2 A and the output is given in Figure 5.9c. The amplitude of limit cycle oscillation is 50 mV at 29.76 kHz. It is evident from the plots that for a digitally controlled DC-DC converter with low resolution ADC (6-bit) and DPWM (7-bit), the Kalman filter has reduced the limit cycle oscillation.

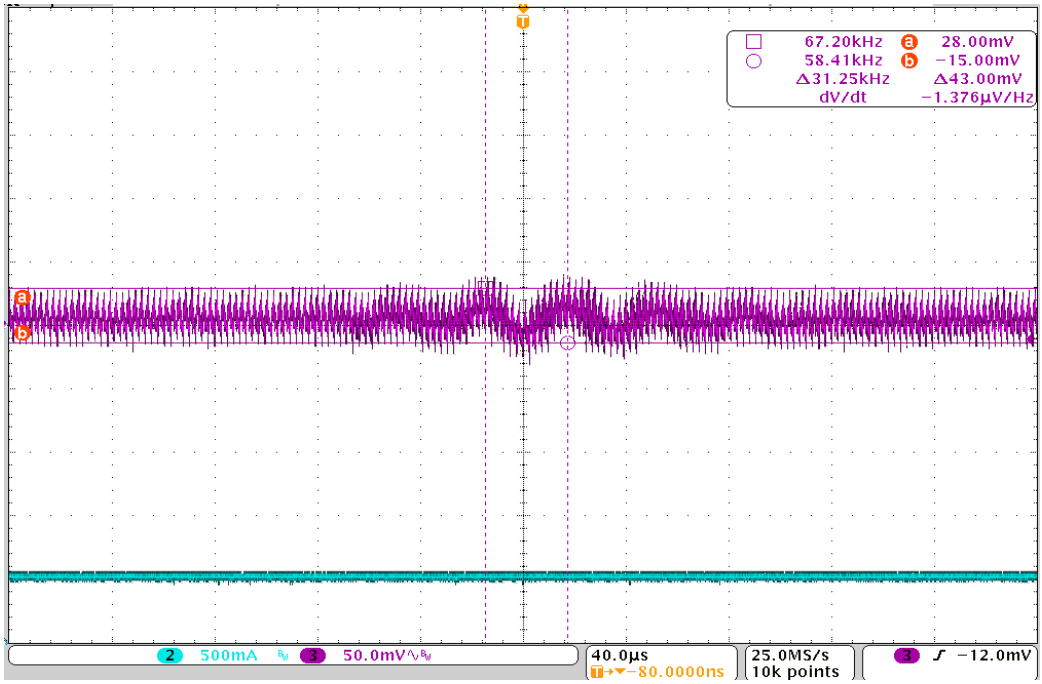

Figure 5.9a: Output of the converter with Kalman Filter (purple trace), Input voltage of 18 V and load condition of 500 mA. Load current is shown by blue trace.

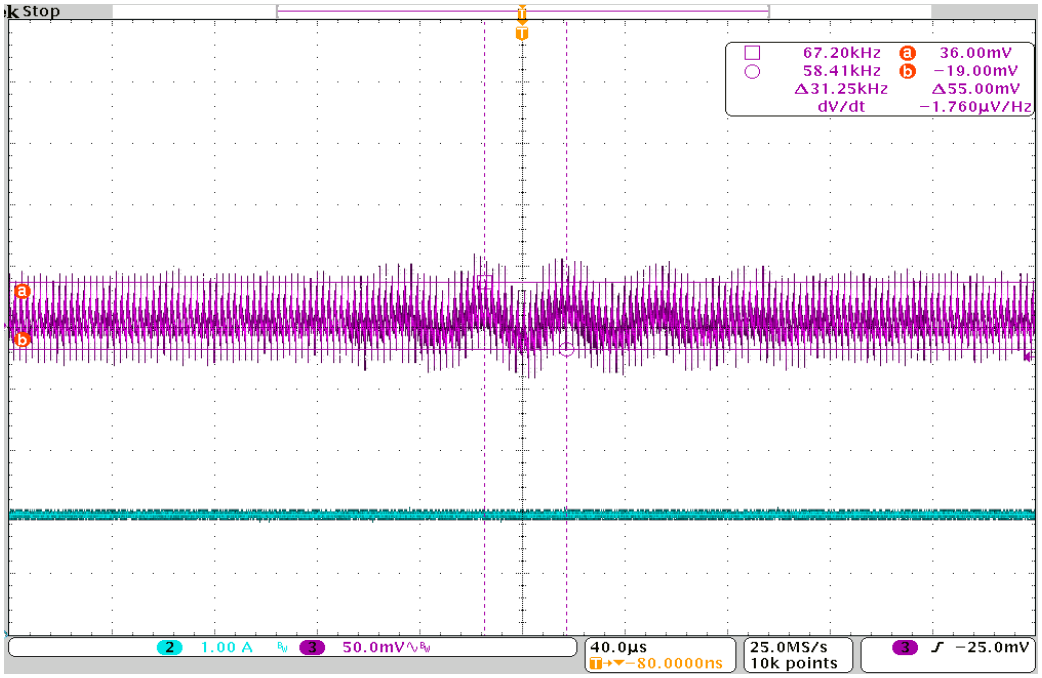

Figure 5.9b: Output of the converter with Kalman Filter (purple trace), Input voltage of 18 V and load condition of 2 A. The load current is shown by blue trace.

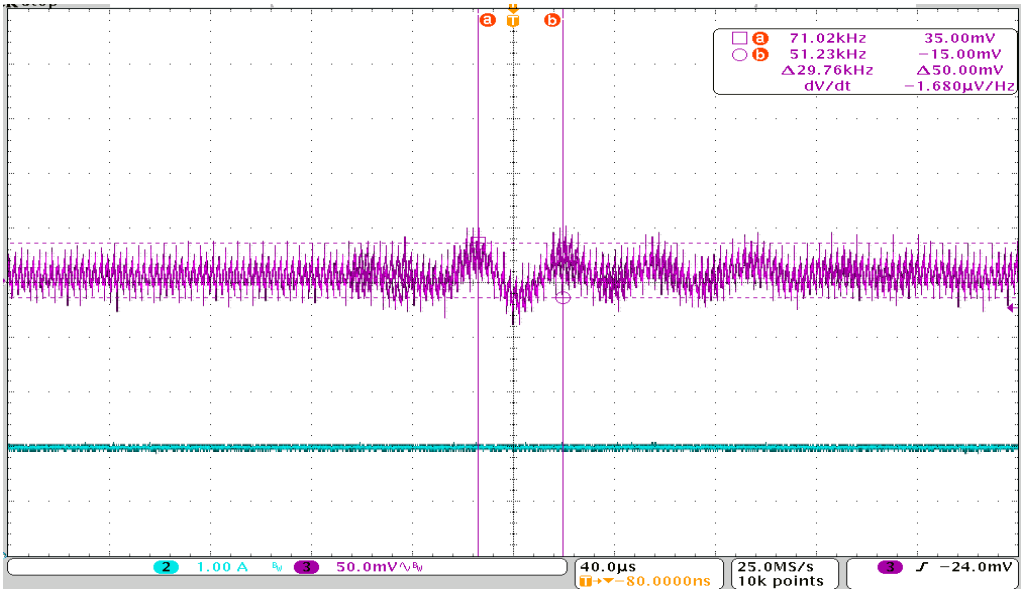

Figure 5.9c: Output of the converter with Kalman Filter (purple trace), Input voltage of 12 V and load condition of 2A. The load current is shown by blue trace.

In the third case, only QEC was introduced to correct the quantization error of DPWM. The input voltage is 18 V and the load current is 500 mA. The limit cycle oscillation is 65 mV at frequency of 3 kHz and the plot is given in Figure 5.10a. The load is changed to 2 A and the plot is shown in Figure 5.10b. The amplitude of limit cycle oscillation is 66 mV at 4.125 kHz. The input voltage is changed to 12 V and the load condition is set at 2 A and the amplitude of limit cycle oscillation is 50 mV at 2.9 kHz. It is evident from the plots that for a digitally controlled DC-DC converter with low resolution ADC (6-bit) and DPWM (7-bit), the QEC has reduced the limit cycle oscillation.

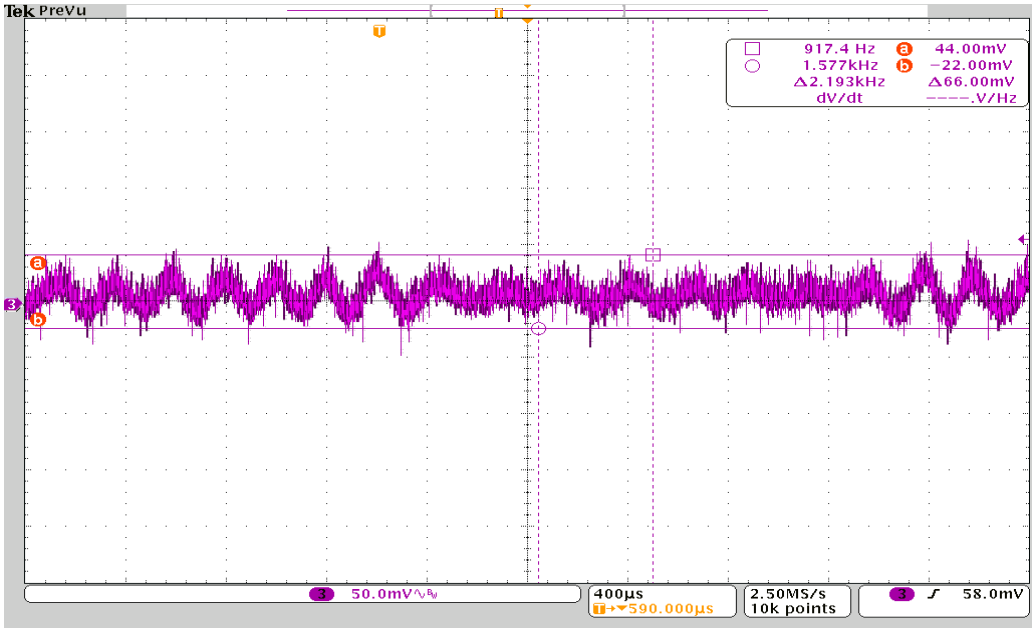

Figure 5.10a: Output of the converter with QEC. Input voltage of 18 V and load condition of 500 mA

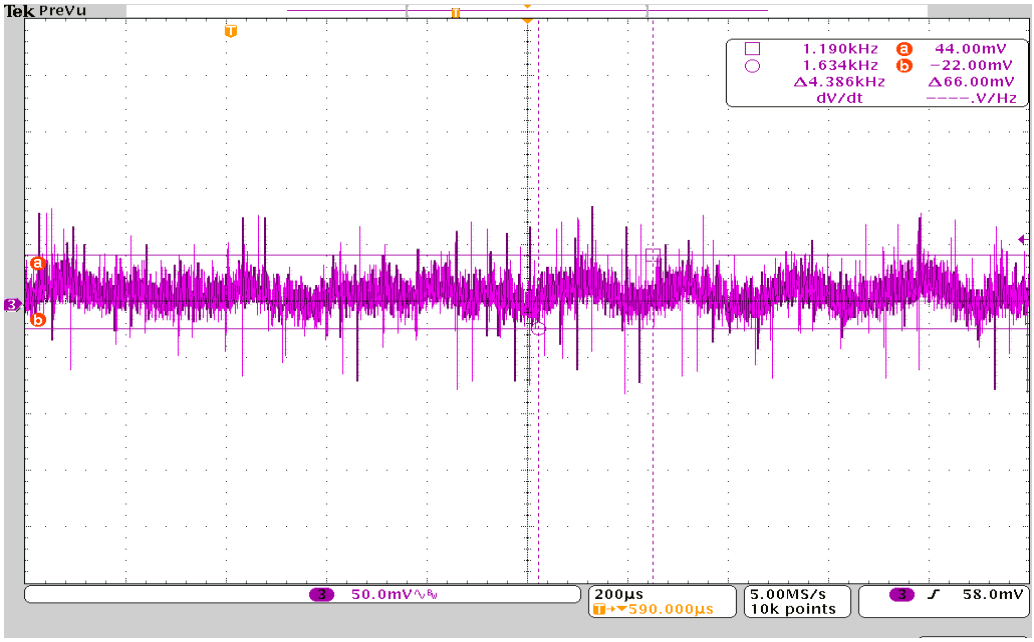

Figure 5.10b: Output of the converter with QEC. Input voltage of 18 V and load condition of 2A

In the fourth case, both QEC and Kalman filter was introduced to correct the quantization error due to ADC and DPWM. The test was repeated for input voltage of 18 V and the load current is 500 mA. The load was then changed to 2 A and then the input voltage was changed to 12 V. In all the three cases, the output

ripple was 20 mV at 400 kHz as shown in Figure 5.11. The line regulation is 0.82 % and load regulation is 0.345 %.

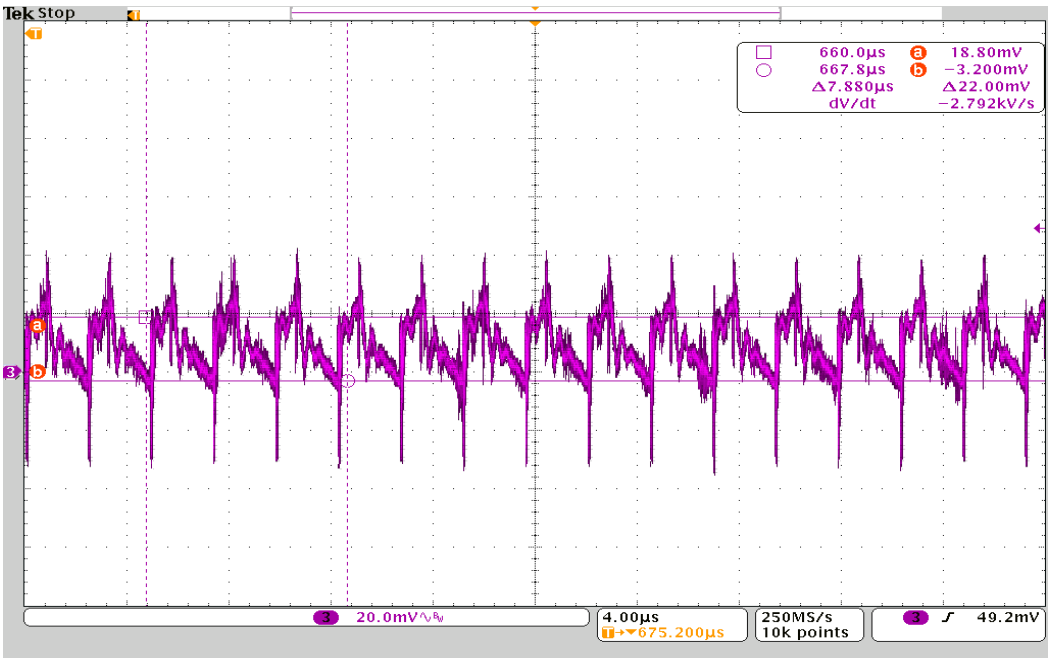

Figure 5.11: Output of the converter with Kalman filter and QEC

The test was repeated for 5-bit ADC and 6-bit DPWM. The switching waveform was jittery. Thus it is seen that up to 6-bit ADC and 7-bit DPWM the test has given satisfactory performance. In the simulation the truncation error due to the fixed point processor has not been accounted and hence there is a difference with the practical results.

5.4 Conclusion

A most appropriate configuration for a digitally controlled DC-DC converter with reduced hardware has been arrived at by combining the advantages of the Kalman filter and QEC. With 6-bit ADC and 7-bit DPWM, the converter meets all specifications without any limit cycle oscillation. A reduced state Kalman filter gives the optimum estimate of the change in output voltage from the noisy measurement from the ADC and the quantization error due to DPWM is corrected by adjusting the switching frequency.

CHAPTER 6

Conclusions and Future Scope

6.1 Conclusion

For the practical implementation of digitally controlled DC-DC converter, a high resolution ADC and high resolution DPWM are required to achieve tight regulation and to avoid undesirable quantization effects such as limit cycle oscillation. The thesis investigated a method to reduce the limit cycle oscillation due to low resolution ADC in digitally controlled DC-DC converter. A novel method to reduce the limit cycle oscillation using reduced state Kalman filter was proposed. The reduced state Kalman filter gives the optimal estimate based on the noisy measurement from ADC and the prediction using small signal model of the converter. Due to state reduction a computational efficient implementation with reduced clock cycle has been possible. The offline computation of the Kalman gain has also facilitated the reduction in clock cycle. The simulation and experimental results show that the proposed scheme had reduced the limit cycle oscillation completely for different resolutions of ADC in a more computationally efficient approach. It was also proved experimentally that the Kalman gain computed offline was effective for all input voltage and load variations. Using the proposed scheme, a coarse ADC can be used in a digitally controlled DC-DC converter without affecting the performance.

A high resolution DPWM, with resolution more than of ADC is required to avoid limit cycle oscillation [3] [4]. Software methods such as dithering and sigma delta modulation scheme have been used to improve the effective resolution of DPWM. This work aims at the usage of a low resolution DPWM without affecting the performance and at the same time significantly reducing limit cycle oscillation. The software method reported in [3] increases the effective resolution of the DPWM but does not improve the conducted emissions from the converter. In this work efforts are made to improve the conducted emission also. Conventional PWM converters exhibit high conducted emissions at the fundamental switching

frequency and its harmonics. Conducted emission noise of the converter can be mitigated by the modulation of the switching frequency. By the frequency modulation of switching frequency, the harmonic peaks are lowered even though it results in more sidebands spaced by the modulating frequency. By further introducing randomness in switching frequency generation, the harmonic power can significantly come down compared to FM and conventional PWM.

The thesis has further investigated a new scheme that combines the advantages of frequency modulation of switching frequency and the sigma delta modulation scheme used to improve the effective resolution of DPWM. In the proposed scheme the switching frequency is adjusted in the n^{th} cycle such that the duty ratio changes by the number of LSBs corresponding to the quantization error accumulated up to the n^{th} cycle. The change of switching frequency in the n^{th} cycle, for quantization error correction, brings reduction in the ripple due to limit cycle oscillations and in conducted emissions levels. Reduction by 17 dB in the ripple and reduction by 25 dB in the conducted emission level has been achieved. This scheme has significant advantage over sigma delta DPWMs as the conducted emission levels have also been drastically reduced in addition to the improvement in the effective resolution.

The thesis proposes a configuration for the digital controller with low resolution ADC and DPWM by combining the advantages of both the schemes. The reduced state Kalman filter gives the optimum estimate of the output voltage from the noisy measurement from low resolution ADC and the QEC by frequency adjustment improves the effective resolution of DPWM. A 6-bit ADC with 7-bit DPWM was simulated for various input and output voltages. The comparison between different schemes was simulated. The different schemes are 1) with no correction for limit cycle oscillation 2) with reduced state Kalman 3) with quantization error correction 4) Quantization error correction for low resolution DPWM and reduced Kalman filter. A 6-bit ADC and 7-bit DPWM gives very good performance with both the schemes combined together. Line regulation of 0.85 %, load regulation of 0.1 % with ripple of around 20 mV at the switching frequency has been achieved. The limit cycle oscillation has been drastically reduced by

combining the above schemes. Thus by combining two schemes, a low resolution ADC with 6-bit resolution and 7- bit DPWM has been used in a digitally controlled DC-DC converter without any limit cycle oscillations and performance degradation. This is the most appropriate configuration keeping in view of the requirement of reducing the output ripple in practical situations.

6.2 Future scope

The present study has been considered for a buck topology. All the above mentioned schemes can be implemented in boost, buck boost, forward, flyback and push pull topology also. The scheme of improving the limit cycle oscillation due to low resolution DPWM can be further improved by considering Numerically Controller Oscillator (NCO) based DPWM instead of counter based DPWM. NCO based DPWM gives better results as it has linear control over switching frequency.

By combining the reduced state Kalman filter and the quantization error correction, an area efficient ASIC with the optimal configuration can be implemented. As the resolution of the DPWM is improved by the correction of quantization error, the implementation of 7-bit DPWM for a DC-DC converter with switching frequency 400 kHz requires only clock frequency of 51.2 MHz. Also, as the clock frequency has been reduced the high frequency interferences will be drastically reduced. The chip area will also come down due to the realization of 6-bit ADC.

REFERENCES

[1] A.V. Peterchev, J. Xiao, and S.R. Sanders," Architecture and IC implementation of a digital VRM controller", IEEE Transactions on Power Electronics, Special Issue on Digital Control, vol. 18, pp. 356-364, January 2003.

[2] B. Patella, A. Prodic, A. Zirger and D. Maksimovic, "High-frequency digital controller PWM controller IC for DC-DC converters", IEEE Transactions on Power Electronics, Special Issue on Digital Control, vol.18, pp. 438-446, January 2003.

[3] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters", IEEE Transactions on Power Electronics, vol. 18, no. 1, pp. 301–308, Jan. 2003.

[4] H. Peng, A. Prodic, E. Alarcon and D. Maksimovic, "Modeling of quantization effects in digitally controlled DC–DC converters", IEEE Transactions on Power Electronics, vol. 22, no. 1, pp. 208–215, Jan. 2007.

[5] Yan-Fei Liu, Eric Meyer and Xiaodong Liu, "Recent developments in digital control strategies for DC/DC switching power converters", IEEE Transactions on Power Electronics, vol. 24, no.11, pp. 2567-2577, Nov 2009.

[6] D. Maksimovic, R. Zane, and R. Erickson, "Impact of digital control in power electronics", Proc. IEEE Int. Symp. Power Semiconductor Devices ICs, pp. 13–22, 2004.

[7] Amir Parayandeh and Aleksandar Prodic, *"Programmable* analog-to-digital converter for low-power DC–DC SMPS", IEEE Transactions on Power Electronics, vol. 23, no. 1, pp. 500-505, Jan 2008.

[8] H. Haita, O, V. Yousefzadeh and D. Maksimovic, “Non-uniform A/D quantization for improved dynamic responses of digitally controlled DC–DC converters”, IEEE Transactions on Power Electronics, vol. 23, no. 4, pp. 1998 – 2005, 2008.

[9] A. P. Dancy and A. P. Chandrakasan, “Ultra low power control circuits for PWM converters”, IEEE Power Electronics Specialists Conference, pp. 21–27, June 1997.

[10] A. Syed, E. Ahmed, D. Maksimovic, and E. Alarcon, “Digital pulse width modulator architectures”, Proc. 35th Annual IEEE Power Electronics Specialists Conference, vol. 6, pp. 4689–4695, June 2004.

[11] Vahid Yousefzadeh, Toru Takayama and Dragan Maksimovic, “Hybrid DPWM with digital delay-locked loop”, Proceedings IEEE Workshop on Computers in Power Electronics (COMPEL), pp. 142 – 148, July 2006.

[12] S.C. Huerta, A. de Castro, O. Garcia and J.A Cobos, “FPGA based digital pulse width modulator with time resolution under 2 ns”, IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 3135–3141, November 2008.

[13] O. Trescases, W. Guowen and T. Wai, “A segmented digital pulse width modulator with self–calibration for low–power SMPS”, IEEE Electron Devices and Solid-State Circuits Conference, pp. 367–370, 2005.

[14] Anthony Kelly and Karl Rinne, “High resolution DPWM in a DC–DC converter application using digital sigma delta techniques”, Power Electronics Specialist conference, IEEE 36th, pp. 1458-1463, 2005.

[15] Zhengyu Lu, Zhaoming Qian, Yong Zeng, Wenxi Yao, Guozhu Chen and Yousheng Wang, “Reduction of digital PWM limit ring with novel control algorithm”, Proceedings 16th Annual IEEE Applied Power Electronics Conference and Exposition, vol. 1, pp. 521-525, 2001.

[16] Z. Lukic, N. Rahman and A. Prodic, “Multibit Σ–Δ PWM digital controller IC for DC–DC converters operating at switching frequencies beyond 10 MHz”, IEEE Transactions on Power Electronics, vol. 22, no. 5, pp. 1693 – 1707, 2007.

[17] J. Li, Y. Qiu, Y. Sun, B. Huang, M. Xu, Dong S. Ha and F.C. Lee, “High Resolution Digital Duty Cycle Modulation Schemes for Voltage Regulators”, Proc. IEEE 22nd Applied Power Electronics Conf. (APEC’07), pp. 871–876, 2007.

[18] S. Saggini, P. Mattavelli, G. Garcea and M. Ghioni, “A Mixed-Signal Synchronous/Asynchronous Control for High-Frequency DC-DC boost Converters”, IEEE Transactions on Industrial Electronics, vol. 55, no. 5, pp. 2053 – 2060, 2008.

[19] V. Yousefzadeh, W. Narisi, Z. Popovic, and D. Maksimovic, “A digitally controlled DC/DC converter for an RF power amplifier”, IEEE Transactions on Power Electronics, vol. 21, no. 1, pp. 164–172, Jan. 2006.

[20] D. Maksimovic, and Regan Zane, “Small-signal discrete-time modeling of digitally controlled PWM converters”, IEEE Transactions on Power Electronics, vol. 22, no.6, pp. 2552-2556, Nov. 2007.

[21] D. M. Van de Sype, K. De Gusseme, F. M. L. L. De Belie, A. P. Van den Bossche, and J. A. Melkebeek, “Small-signal z-domain analysis of digitally controlled converters”, IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 470–478, Mar. 2006.

[22] M. M. Peretz and S.B. Yaakov, “Time-domain design of digital compensators for PWM DC-DC converters”, IEEE Transactions on Power Electronics, vol. 27, no.1, pp. 284-293, Jan. 2012.

[23] M.G. Rajesh Kumar, G. Sajitha and Thomas Kurian, “Digital control of multiple output DC-DC converter using 16 bit microcontroller”, International Journal of Power electronics, vol. 3, no. 3, pp. 225-238, 2011.

[24] C. Yuen Fong, M. Moallem and W. Wang, “Design and implementation of modular FPGA-based PID controllers”, IEEE Transaction on Industrial Electronics, vol. 54, no. 4, pp. 1898 – 1906, 2007.

[25] Prodic, A. Maksimovic, D. and Erickson, R.W., "Design and implementation of a digital PWM controller for a high-frequency switching DC-DC power converter", IECON '01, The 27th Annual Conference of the IEEE Industrial Electronics Society, vol. 2, pp. 893-898, 2001.

[26] Alejandro R. Oliva, Simon S. Ang, and G. E. Bortolotto**,** “Digital Control of a voltage-mode synchronous buck converter”, IEEE Transactions on Power Electronics, vol. 21, no. 1, pp. 157–163, Jan. 2006.

[27] J. Xiao, A. Peterchev, J. Zhang, S. Sanders, “An ultra-low-power digitally-controlled buck converter IC for cellular phone applications”, in Proc. IEEE 19th Applied Power Electronics Conf. (2004), vol. 1, pp. 383–391, 2004.

[28] M. Milanovic, M. Truntic, and P. Slibar, “FPGA implementation of digital controller for DC-DC buck converter”, Proc. 5th Int. Workshop Syst.-On-Chip Real-Time Appl., pp. 439–443, July 2005.

[29] A. Barrado, J. Quintero, A. Lazaro, C. Fernandez, P. Zumel, and E. Olias, “Linear-non-linear control applied in multiphase VRM”, Proc. IEEE 36th Annu. Power Electron. Spec. (PESC’05), pp. 904–909, 2005.

[30] G. Feng, E Meyer and Yan-Fei Liu, “A new digital control algorithm to achieve optimal dynamic performance in DC-to-DC converters”, IEEE Transactions on Power Electronics, vol. 22, no. 4, pp. 1489-1498, July 2007.

[31] Z. Zhao and A. Prodic, " Continuous - time digital controller for high frequency DC–DC converters", IEEE Transactions on Power Electronics, vol. 23, no.2, pp. 564–573, Mar. 2008.

[32] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcón, L. Pao and Dragan Maksimovic, "Proximate time-optimal digital control for synchronous buck DC–DC converters", IEEE Transactions on power electronics, vol. 23, no.4, pp. 2018-2025, July 2008

[33] A Babazadeh and Dragan Maksimovic, "Hybrid digital adaptive control for fast transient response in synchronous buck DC–DC converters", IEEE Transactions on power electronics, vol. 24, no.11, pp. 2625-2638, Nov. 2009.

[34] A. Barrado, R. Vazquez, A. Lazaro, J. Pelite, and E. Olias, "Fast transient response with combined linear-non-linear control applied to buck converters", IEEE 33rd Annual Power Electronics Specialists Conference (PESC'02), vol. 4, pp. 1587-1592, June 2002.

[35] A. Barrado, A. Lazaro, J. Pelite, R.Vazquez, and E. Olias "Linear non- linear control (LnLc) for DC/DC buck converters: stability and transient response analysis", 9th Annual IEEE Applied Power Electronics Conference and Exposition (APEC'04), vol. 2, pp. 1329- 1335, February 2004.

[36] E.V. Idiarte, A.M. Pastor, G. Garcia, A.C. Pastor, L.M. Salamero,"Discrete-time sliding-mode-based digital pulse width modulation control of boost converter", IET Power Electronics, vol.8, Iss.5, pp. 708-714, 2015

[37] Albert T.L. Lee, Johnny K.O. sin and Philip C.H. Chan, "Adaptive high-bandwidth digitally controlled buck converter with improved line and load transient response", IET power electronics, vol.7, Iss. 3, pp. 515-525, 2014.

[38] P. Mattavelli, L. Rossetto, G. Spiazzi and P. Tenti, “General purpose fuzzy controller for DC-DC converters”, IEEE Transactions on Power Electronics, vol. 12, Issue 1, pp.79 – 86, Jan 1997.

[39] T. Gupta, R. R. Boudreaux, R. M. Nelms and J. Y. Hung, “Implementation of a fuzzy controller for DC-DC converters using an inexpensive 8-b microcontroller”, IEEE Transactions on Industrial Electronics, vol. 44, Issue 5, pp. 661-669, Oct 1997.

[40] A. G. Perry, G. Feng, Y.-F. Liu, and P. C. Sen, “A design method for PI-like fuzzy logic controllers for DC–DC converter”, IEEE Transactions on Industrial Electronics, vol. 54, no. 5, pp. 2688–2696, Oct. 2007.

[41] Botao Miao, Regan Zane and Dragan Maksimovic, “System identification of power converters with digital control through cross-correlation methods”, IEEE Transactions on power electronics, vol. 20, no.5, pp. 1093-1099, Sep 2005.

[42] M Shirazi, J. Morroni, A. Dolgov, Regan Zane, and Dragan Maksimovic, “Integration of frequency response measurement capabilities in digital controllers for DC–DC converters”, IEEE Transactions on power electronics, vol. 23, no.5, pp. 2524-2534, Sep 2008.

[43] Botao Miao, Regan Zane and Dragan MaksimoviC, “FPGA based digital network analyzer for digitally controlled SMPS”, IEEE COMPEL Workshop, pp. 240-245 July 16-19, 2006

[44] L. Corradini, P. Mattavelli, and D. Maksimovic, “Robust relay-feedback based auto tuning for DC-DC converters”, Proceedings IEEE Power Electronics Specialist Conference, pp. 2196–2202, June 2007.

[45] J Morroni, R. Zane, and D. Maksimovic, “An online stability margin monitor for digitally controlled switched-mode power supplies”, IEEE transactions on power electronics, vol. 24, no. 11, pp. 2639-2648, Nov 2009.

[46] R. D. Middlebrook, “Measurement of loop gain in feedback systems”, Int. J. Electron., vol. 38, pp. 485–512, 1975.

[47] L. Corradini, P. Mattavelli, W. Stefanutti, and S. Saggini, “Simplified model reference-based auto tuning for digitally controlled SMPS”, IEEE transactions on power electronics, vol. 23, no. 4, pp. 1956–1963, Jul. 2008.

[48] Mariko Shirazi, Regan Zane and Dragan Maksimovic, “ An auto tuning digital Controller for DC–DC power converters based on online frequency-response measurement”, IEEE Transactions on Power Electronics, vol. 24, no.11, pp. 2578-2587, Nov 2009.

[49] J. Morroni, R. Zane and Dragan Maksimovic, “Design and implementation of an adaptive tuning system based on desired phase margin for digitally controlled DC–DC converters”, IEEE Transactions on power electronics, vol. 24, no.2, pp. 559-564, Feb 2009.

[50] J. Morroni, L. Corradini, R. Zane and D. Maksimovic, “Adaptive tuning of switched-mode power supplies operating in discontinuous and continuous conduction modes”, IEEE Transactions on power electronics, vol. 24, no.11, pp. 2603-2611, Nov. 2009.

[51] Feng Lin and Dan Y. Chen, “Reduction of power supply EMI emission by switching frequency modulation”, IEEE Transactions on Power Electronics, vol. 9, no. 1, pp. 132-137, January 1994.

[52] David Gonzalez, Josep Balcells, Alfonso Santolaria, Jean-Charles Le Bunetal, Javier Gago, Didier Magnon, and Stephane Brehaut. “Conducted EMI reduction in power converter’s by means of periodic switching frequency modulation”, IEEE Transactions on Power Electronics, vol. 22, no. 6, pp. 2271-2281, Nov. 2007.

[53] K. K. Tse, Henry Shu-Hung Chung, S. Y. Ron Hui, and H. C. So, “A comparative study of carrier-frequency modulation techniques for

conducted EMI Suppression in PWM converters", IEEE Transactions on Industrial Electronics, vol. 49, no.3, pp. 618-627, June 2002.

[54] K.K Tse, Henry Shu-Hung Chung, S.Y. Hui and H.C. So," Analysis and spectral characteristics of a spread-spectrum technique for conducted EMI suppression", IEEE Transactions on Power Electronics, vol.15, no. 2, pp. 399-410, March 2000.

[55] Oliver Trescases, Guowen Wei, Alexander Prodic and Wai Tung Ng," An EMI reduction technique for digitally controlled SMPS", IEEE Transactions on Power Electronics, vol. 22, no. 4, pp. 1560-1565, July 2007.

[56] S. Y. (Ron) Hui, Yash Shrivastava, S. Sathiakumar, K. K. Tse, and Henry Shu-Hung Chung, "A comparison of nondeterministic and deterministic switching methods for DC–DC power converters", IEEE Transactions on Power Electronics, vol. 13, no. 6, pp. 1046-1055, Nov. 1998.

[57] K. K Tse, R. Wai-Man Ng, HenryShu-Hung Chung, and S.Y. RonHui, "An evaluation of the spectral characteristics of switching converters with chaotic carrier-frequency modulation", IEEE Transactions on Industrial Electronics, vol.58, no.1, pp. 171-182, Feb. 2003.

[58] Alfonso Santolaria, "Effects of switching frequency modulation on the power converter's output voltage", IEEE Transactions on Industrial Electronics, vol .56, no.7, pp. 2729-2737, Jul 2009.

[59] J. Xu and J. wang, "Bifrequency pulse train control technique for switching DC-DC converters operating in DCM with fast transient response and low EMI", IEEE Transactions on Power Electronics, vol. 58, no. 8, pp. 3658-3667, Aug. 2011.

[60] J. Xang and J. Xu, "Peak current mode Bifrequency control technique for switching DC-DC converters operating in DCM", IEEE Transactions on Power Electronics, vol. 27, no. 4, pp. 1876-1884, April. 2012.

[61] Fabio Pareschi, G. Setti, R. Rovatti and G. Frattini, “Practical optimization of EMI Reduction in spread spectrum clock generators with application to switching DC/DC converters”, IEEE Transactions on Power Electronics, vol. 29, no. 9, pp. 4646-4657, Sep. 2014.

[62] S. Kapat, “Reconfigurable Periodic Bifrequency DPWM with custom harmonic reduction in DC-DC Converters”, IEEE Transactions on Power Electronics, vol. 31, no.49, pp. 33803368, April 2016.

[63] Steven.M. Kay, “Fundamentals of Statistical Signal Processing: Estimation Theory”, Volume 1, Prentice Hall, New Jersey, 1993.

[64] Darrell Williamson, “Finite word length design of digital Kalman Filters for state estimation”, IEEE Transactions on Automatic Control**, v**ol. 30, no.10, pp. 930-939, 1985.

[65] H. Cho, S.Y. Yoo and S. Kwak, “State observer based sensor less control using Lyapunov's method for boost converters”, IET Power Electronics, vol.8, Iss.1, pp. 11-19, 2015.

[66] Daniel Luong-Van, Michal J. Tordon and Jayantha Katupitiya, “Covariance profiling for an adaptive Kalman Filter to suppress sensor quantization effects”, IEEE Conference on Decision and Control, vol. 3, pp. 2680-2685, 2004.

[67] Jian XU, Jianxun LI , Sheng XU2, “Analysis of quantization noise and state estimation with quantized measurements”, Journal of Control Theory Applications, vol. 9, no.1, pp. 66–75, 2011.

[68] B. Widrow and I. Kollar, “Quantization Noise: Round off Error in Digital Computation, Signal Processing, Control, and Communications”, Cambridge University press, New York, 2008.

[69] M. G. Y. Batarseh, “Digital pulse width modulator techniques for DC-DC converter", Ph.D. Dissertation, University of Central Florida, Spring Term. 2010.

[70] A. Peterchev, "Digital control of PWM Converters: Analysis and application to voltage regulation modules", MS Dissertation, University of California, Spring 2002.

[71] J. Xiao**,** "An ultra-low-quiescent-current dual-mode digitally-controlled buck converter IC for cellular phone applications", Ph.D. Dissertation, University of California, Fall 2003.

[72] Tao Liu, “Digitally controlled DC-DC buck converters with lossless current sensing," Ph.D. Dissertation, Arizona State University, Dec. 2011.

[73] M. Shirazi, "Embedded frequency response measurement capability for monitoring and tuning of system dynamics in digitally-controlled DC-DC converters", Ph.D. Dissertation, University of Colorado, 2009

[74] J. Wang, "Digitally controlled DC-DC Converters with fast and smooth load transient response", Ph.D. Dissertation, University of Toronto, 2013.

[75] Robert W. Erickson, “Fundamentals of Power Electronics Second Edition”, Second Edition, University of Colorado, 2000

[76] Z. Zhao and A. Prodic, “Limit cycle oscillations based auto-tuning system for digitally controlled DC-DC power supplies”, IEEE Transactions on Power Electronics, vol. 22, no. 4, pp. 2211-2222, Nov. 2007.

[77] L. Corradini, D. Maksimovic, P.Mattavelli and R. Zane, “ Digital control of high-frequuency switched-mode power converters”, IEEE Press, John Wiley & Sons, Inc., New Jersey, 2015

APPENDIX 1

Describing function

In order to analyze the non-linearity due to the quantization effect of ADC and DPWM the describing function method has been selected [4]. Basically, the describing function method can be treated as a linear function for the analysis and it provides an approximation to the behavior of the non-linear system. The describing function, which is a linear function depend on the amplitude and the frequency of the input signal. Successful applications of the describing function method rely on the assumption that the input x to the nonlinearity is sinusoidal i.e.

$$x = a\sin\omega t \tag{A1.1}$$

With such an input, the output of the non-linear element will be in general be non-sinusoidal periodic function which may be expressed in terms of Fourier series as given below

$$y = A_0 + A_1\sin\omega t + B_1\sin\omega t + A_2\sin 2\omega t + B_2\sin 2\omega t + \cdots \tag{A1.2}$$

Assumptions

1. Non linearity N does not generate sub harmonics

2. Nonlinearity is symmetrical, so the average value of y is zero so the output can be written as

$$y = A_1\sin\omega t + B_1\sin\omega t + A_2\sin 2\omega t + B_2\sin 2\omega t + \cdots \tag{A1.3}$$

3. All the harmonics are filtered out as the system has low pass characteristics

$$y = A_1\sin\omega t + B_1\sin\omega t \tag{A1.4}$$

$$y = Y_1\sin(\omega t + \phi) \tag{A1.5}$$

Where the coefficients A_1 and B_1 of the Fourier series are

$$A_1 = \frac{1}{\Pi}\int_0^{2\Pi} y\sin\omega t\, d\omega t \quad \text{(A1.6)}$$

$$B_1 = \frac{1}{\Pi}\int_0^{2\Pi} y\cos\omega t\, d\omega t \quad \text{(A1.7)}$$

The sinusoidal input describing function, denoted N(A), is by definition:

$$N(A) = \frac{\text{phasor representation of output component at frequency}\omega}{\text{phasor representation of input component at frequency}\omega} \quad \text{(A1.8)}$$

Thus the describing function $N(A) = (\frac{Y_1}{a})e^{j\phi}$ (A1.9)

A1.1 Describing function of a quantizer

The idealized characteristics of a non-linearity due to quantization effect and its response to sinusoidal input are shown in Figure A1.1[4]. Consider a quantizer having the characteristic, $y = Q(x)$. The describing function of a quantizer, when the DC offset is $\varepsilon = 0$, i.e., the DC value of the input sinusoidal signal matches the midpoint of a quantization bin is shown in Figure A1.1

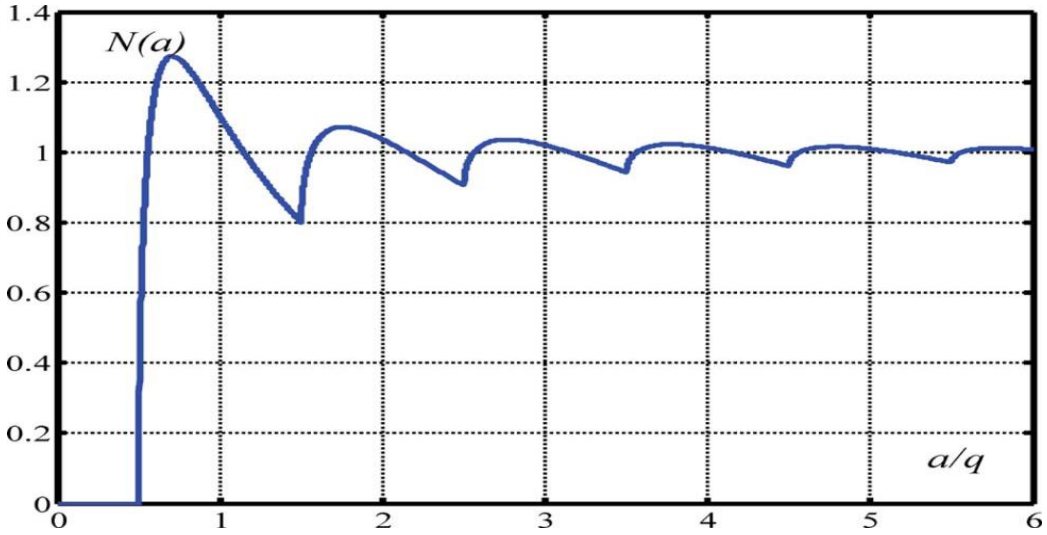

Figure A1.1: Describing function of a quantizer when the DC offset is $\boldsymbol{\varepsilon = 0}$, i.e., the DC value of the input sinusoidal signal matches the midpoint of a quantization bin. [4]

Figure A1.1 shows the textbook result for the describing function of a quantizer. Notice that the maximum effective gain of $\frac{4}{\Pi} = 1.27$ is obtained for $a = \frac{q}{\sqrt{2}}$, and that approaches 1 for a >> q.

The describing function of a quantizer depends not only on the amplitude of the assumed sinusoidal input signal, but also on the input signal DC offset with respect to the mid-point of a quantization bin [4]. Assuming that

$$x = \varepsilon + a\sin\omega t \tag{A1.9}$$

The amplitude and offset dependent "gain" of a quantizer can be significantly greater than one as the offset ε approaches $\frac{q}{2}$. In the worst case, $\varepsilon = q/2$, the input sinusoidal signal is centered at the transition point of the quantizer. Figure A1.2 shows an example of the input and output

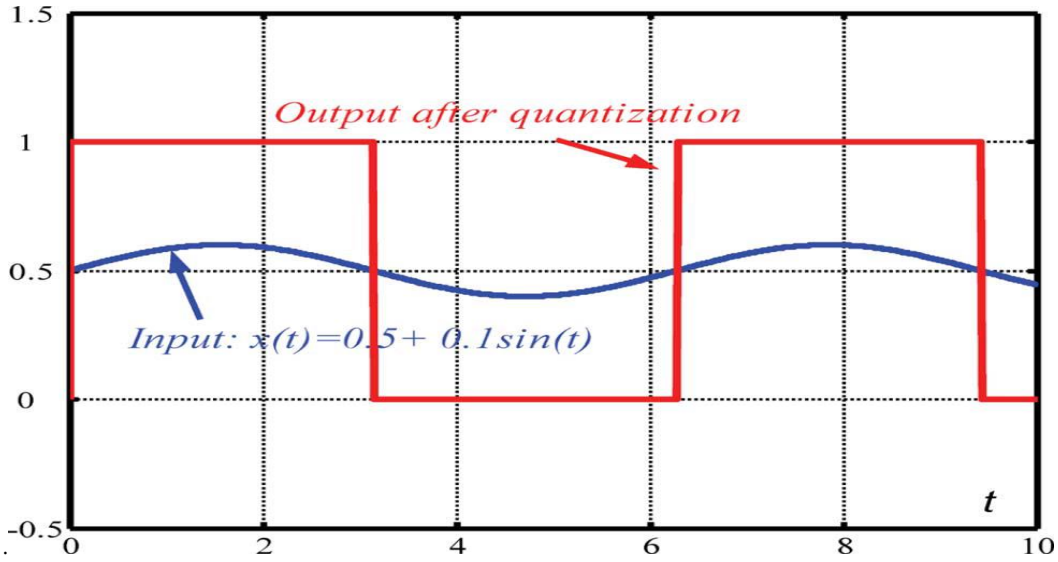

Figure A1.2: Small amplitude sinusoidal signal becomes square wave signal with much bigger amplitude when the DC offset $\boldsymbol{\varepsilon}$ of the input sinusoidal signal matches the transition point $(0.5q)$ between two quantization bins [4]

The describing function of the input sinusoidal signal with dc offset is shown in Figure A1.3. The input signal with small amplitude can produce an output greater than one and if the offset ε is equal to q/2 then the effective gain can be infinitely large. In the case with low resolution ADC where the reference voltage is selected in such a way that it does not coincide with the zero error bin, the offset will also result.

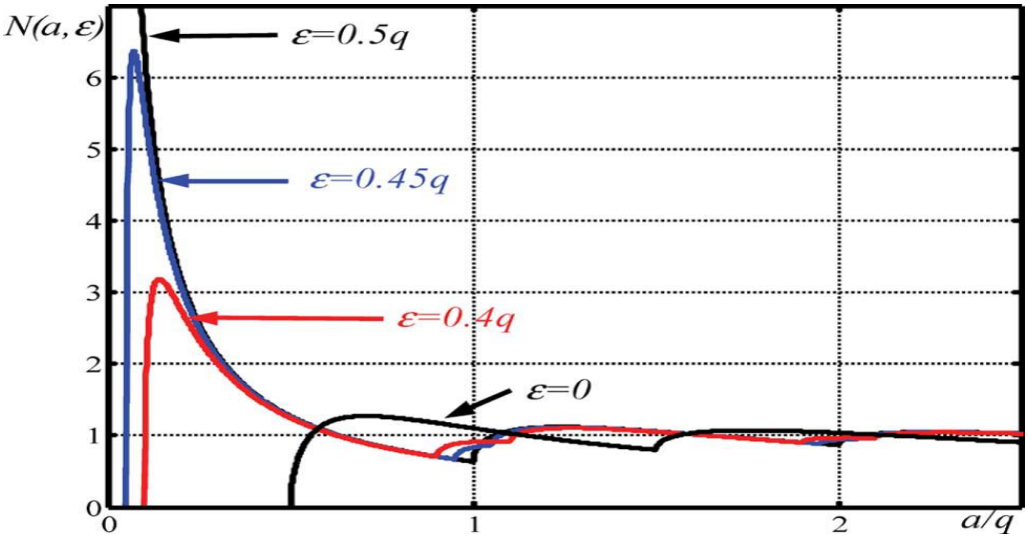

Figure A1.3: Describing function of a quantizer for several different values of the offset

A1.2 Relationship between limit cycle oscillation and load resistance

The relationship between limit cycle oscillation and load resistance is given in [76]. The amplitude (A_{LC}) and frequency (f_{LC}) of the limit cycle oscillation can be found from the following equation.

$$-1 = 1 < 180^{\circ} = N_{DPWM}(A_{LC}, \varepsilon) G_{vd}(j\omega_{LC}) K_{ADC}(j\omega_{LC}) K_{PID}(j\omega_{LC}) \quad \text{(A1.10)}$$

where $N_{DPWM}(A_{LC}, \varepsilon)$ describes the gain of the DPWM, $G_{vd}(j\omega_{LC})$ is control-to-output transfer function of the switching converter, $K_{PID}(j\omega_{LC})$ is the transfer function of the compensator and $K_{ADC}(j\omega_{LC})$ is input-to-output transfer function of the ADC. Also, to simplify the analysis we assume that the frequency of LCO is much smaller than the switching frequency and that, at f_{LC}, the delays of ADC and DPWM have negligible effects.

$N_{DPWM}(A_{LC}, \varepsilon)$, the gain of the DPWM, depends not only on the amplitude of the input signal but also on the offset of the input signal. Let us assume that the offset is zero. Then the gain of the DPWM can be given by

$$N_{DPWM}(A_{LC}) = \frac{4q_{dpwm}}{\pi A_{LC}} \quad \text{(A1.11)}$$

The control to output transfer function for a buck converter is given by [76]

$$G_{vd}(s) = V_{in}\frac{1}{1+\frac{s}{Q\omega_0}+\frac{s^2}{{\omega_0}^2}} \quad \text{(A1.12)}$$

where q_{dpwm} is the quantization step of DPWM ($q_{dpwm} = \frac{V_m}{2^{n_{dpwm}}}$), V_m is the voltage range of the DPWM, $\omega_0 = 1/\sqrt{LC}$, $Q = R\sqrt{\frac{L}{C}}$. The output capacitance, inductance and load resistance are indicated by C, L and R. V_{in} is the input voltage. To simplify the analysis, without losing the generality, let us assume that K_{ADC} and K_{PID} is one. Ideally the frequency of the limit cycle oscillation will correspond to the output filter corner frequency ω_0 at which the phase shift of the loop gain is 180º. In practice, this frequency is a little bit lower due to the phase shifts introduced by the delays of ADC and DPWM

The peak to peak amplitude of the limit cycle oscillation is

$$A_{pp} = \frac{4q_{dpwm}}{\pi}\, G_o \frac{R}{w_0 L} \quad \text{(A1.13)}$$

where $G_o = V_{in}$. For very light loads a high value of Q factor could result in excessive limit cycle oscillations.

APPENDIX 2

Design guideline for the computation of Kalman gain

The steps involved in the computation of Kalman filter is given below

1. Compute the measurement noise variance $(\sigma_v{}^2)$ as given below

$$q_{adc} = \frac{V_m}{2^{n_{adc}}} \tag{A2.1}$$

$$\sigma_v{}^2 = \frac{q_{adc}{}^2}{12} \tag{A2.2}$$

2. Compute the process noise variance $(\sigma_w{}^2)$ as given in section A 2.1
3. Compute the minimum prediction mean square error for $(n-1)$ observations, $P(n/(n-1))$ as given below

$$P(n/(n-1)) = a_4{}^2 P((n-1)/(n-1)) + \sigma_w{}^2 \tag{A2.3}$$

4. Compute the Kalman gain $k(n)$ as given below

$$k(n) = \frac{P(n/(n-1))c}{c^2 P((n-1)/(n-1)) + \sigma_v{}^2} \tag{A2.4}$$

5. Compute the minimum mean square error estimation for n observations, $P(n/n)$ as given below

$$P(n/n) = ((1-k(n)c)P(n/(n-1)) \tag{A2.5}$$

c and a_4 are explained in chapter 3.

As measurement noise variance changes with the resolution of ADC and process noise variance changes with the resolution of ADC and DPWM, the Kalman gain varies with the resolution of ADC and DPWM.

A2.1 Computation of Process noise variance $(\sigma_w{}^2)$

Quantization noise at the plant output comes from both quantizers, Q1 and Q2. To compute the process noise error variance [64], the two noise sources due to the quantization of ADC and DPWM are injected into the feedback system at the corresponding point and its effect on the output voltage is obtained as shown in

Figure A2.1. The noise injected by ADC (n1) has a mean square value of $\frac{{q_{adc}}^2}{12}$ and the noise injected by DPWM (n2) has a mean square value of $\frac{{q_{dpwm}}^2}{12}$. A 6-bit ADC would have 2^6 quantum steps covering its input range. If the input range of ADC is from zero to 3.3V, then each quantum step is 0.05151($q_{adc} = \frac{3.3}{2^6}$). The quantization noise due to this is equal to $2.255 * 10^{-4}$. Similarly a 11-bit DPWM has a quantization noise of $7.96 * 10^{-8}$ ($q_{dpwm} = 1/1023$).

The corresponding noise sources, n1 and n2 , are injected into the feedback system as shown in Figure A2.1 and propagate at the system output.

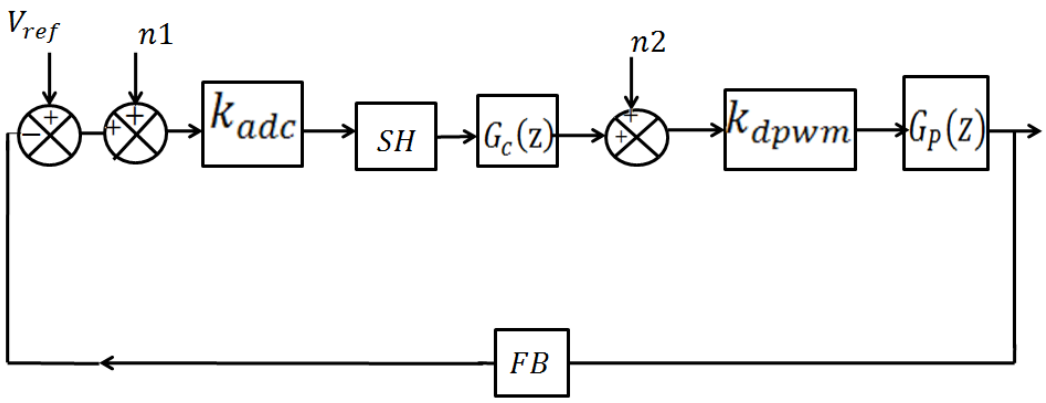

Figure A2.1: System model used for the calculation of process noise

Noise n2 is uncorrelated with noise n1. Since n1 and n2 are uncorrelated with each other, their respective responses at the system output will also be uncorrelated with each other. Hence the mean square of the output quantization noise will be the sum of the mean squares of the noises due to n1 and n2. The two noise components can be calculated separately and then combined.

The transfer function from the point of injection of noise n2 to the system output is given by

$$Gp_{n2}(z) = \frac{G_p(z)\, k_{dpwm}}{1 + G_p(z)\, k_{dpwm}\, SH\, k_{adc}\, FB\, G_c(z)} \qquad \text{(A2.6)}$$

The impulse response is obtained using MATLAB by taking the inverse z transform. The sum of the squares of the impulses of the impulse response from n2 to the system output has been calculated as 8.1186. Accordingly mean square of the output noise due to Q2 is equal to $8.1186 * \frac{{q_{dpwm}}^2}{12}$. Similarly, the transfer function from the point of injection of noise n1 to the system output is computed.

$$Gp_{n1}(z) = \frac{G_p(z)\, k_{dpwm}\, SH\ k_{adc}\, G_c(z)}{1 + G_p(z)k_{dpwm}\, SH\, k_{adc}\, FB * G_c(z)} \qquad \text{(A2.7)}$$

The sum of the squares of the impulses of this impulse response was calculated to be 8.226. Therefore the mean square of the output noise due to Q1 is $8.226 * \frac{{q_{adc}}^2}{12}$ which is equal to $1.855 * 10^{-3}$. The mean of the noise due to Q1 and Q2=$8.226 * 2.255 * 10^{-4} + 8.1186 * 7.96 * 10^{-8}$.

If the non-linearity of ADC and DPWM should be considered then the gain of ADC and DPWM should be multiplied by the corresponding $N(A)$. As explained earlier the value of $N(A)$ for ADC depends on V_{ref}. Hence Kalman gain varies with V_{ref}.

APPENDIX 3

Comparison of Sigma Delta Modulation & Quantization error correction scheme of chapter 4

Both the schemes, the proposed scheme and the sigma delta modulation scheme, increases the effective resolution of the DPWM. In both the schemes, the duty cycle command is pre-processed so that the DPWM quantization noise will be shaped in frequency. The noise at lower frequency is reduced in exchange for more noise at higher frequencies. As a result, the total quantization noise at the output of the DC-DC converter is reduced and the effective resolution of the DPWM in the control loop is increased dramatically. Both the schemes do not affect the stability of the closed loop, because its signal transfer function is unity magnitude and delay free and the closed loop pole is not affected. Both the schemes are explained below.

A3.1 Sigma Delta Modulation

Let $d(n)$ be the duty ratio from the PID controller. $q(n)$ is the quantization noise of DPWM and $d_1(n)$ is the quantized duty cycle. Figure A3.1 shows the sigma delta modulation scheme.

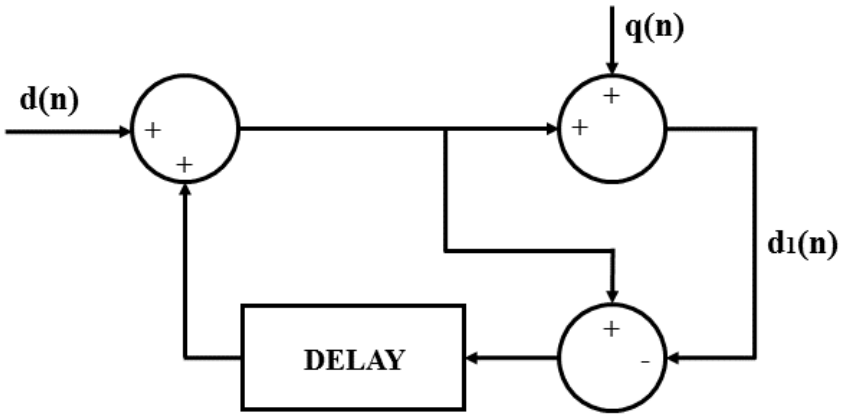

Figure A3.1: Sigma Delta Modulation Scheme

$$d(n) + d(n-1) - d_1(n-1) + q(n) = d_1(n) \quad \text{(A3.1)}$$

$$d(z) + d(z)z^{-1} - d_1(z)z^{-1} + q(z) = d_1(z) \quad \text{(A3.2)}$$

$$d_1(z) = d(z) + \frac{q(z)}{1 + z^{-1}} \tag{A3.3}$$

A3.2 Quantization Error Correction in the n^{th} cycle by changing the switching frequency

For the quantization error correction scheme mentioned in chapter 4, as shown in Figure 4.1, the quantization error is accumulated and is corrected in the n^{th} cycle. In the n^{th} cycle, the duty ratio is given by

$$d(n) + \sum_{m=0}^{n-1} \big(d(m) - d_1(m)\big) + q(n) = d_1(n) \tag{A3.4}$$

Due to the averaging of the output LC filter, the effective duty ratio is

$$\frac{d(1) + d(2) + \cdots + d(n) + \sum_{m=0}^{n-1}\big(d(m) - d_1(m)\big) + nq(n)}{n} = \frac{d_1(1) + d_1(2) + \cdots + d_1(n)}{n} \tag{A3.5}$$

where $d(0) = 0$ and $d_1(0) = 0$

$$\frac{d(1) + (d(0) - d_1(0)) + \cdots + d(n) + (d(n-1) - d_1(n-1)) + nq(n)}{n} = \frac{d_1(1) + d_1(2) + \cdots + d_1(n)}{n} \tag{A3.6}$$

From the equation (A3.6) it is clear that

$$d(n) + \big(d(n-1) - d_1(n-1)\big) + q(n) = d_1(n) \tag{A3.7}$$

$$d_1(z) = d(z) + \frac{q(z)}{1 + z^{-1}} \tag{A3.8}$$

A3.3 Calculation of "n"

In [3], dithering technique has been used to improve the effective resolution of the DPWM and the mathematical derivation for how many bits of dither can be used in a certain system has been presented. As mentioned in chapter 4, the quantization error is corrected in the n^{th} cycle, by changing the switching frequency. Due to this, a new frequency component is generated [3] such that

$$f_n = \frac{f_{sw}}{n} \tag{A3.9}$$

The value of n is to be selected in such a way that the contribution of this content in the ripple is very low. This depends on the amplitude of the new frequency content at the output of the converter. Since the correction is made in the n^{th} cycle, the switching between the two adjacent quantized duty cycle can be modeled as a square wave with worst case peak-to-peak amplitude of $n\Delta V_{dpwm}$, where, $\Delta V_{dpwm} = \frac{V_m}{2^{n_{dpwm}}}$, v_m is the voltage range of the DPWM. It is sufficient to consider the fundamental component of this square wave due to averaging effect of the output LC filter and has an amplitude given by [3]

$$A_{p-p} = \frac{4}{\pi}\frac{nV_m}{2^{n_{dpwm}}} \tag{A3.10}$$

Let $H(f_n)$ be the attenuation at the output LC filter at frequency, f_n. Then the peak to peak output voltage ripple can then be bounded approximately as

$$v_n = H(f_n)A_{p-p} \tag{A3.11}$$

The LC filter has cut off frequency given at $f_0 = \frac{1}{2\pi\sqrt{LC}}$. After this frequency the filter rolls off at -40 dB/decade. The ESR of the output capacitor causes a zero at the frequency, $f_z = \frac{1}{2\pi R_c C}$. The filter characteristics rolls off at -20dB/decade. Thus,

$$\text{for } f_o < f < f_z \quad H(f) \approx \left(\frac{f_0}{f}\right)^2 \tag{A3.12}$$

At $f = \frac{f_{sw}}{n}$

$$v_n \leq \left(\frac{f_0}{f_{sw}}\right)^2 n^3 \frac{4}{\pi} \frac{V_m}{2^{n_{dpwm}}} \tag{A3.13}$$

$$\text{And for } f_o < f_z < f\ , \quad H(f) \approx \left(\frac{f_0}{f_z}\right)^2 \frac{f_z}{f} \tag{A3.14}$$

$$v_n \leq \frac{{f_o}^2}{f_{sw}f_z} n^2 \frac{4}{\pi} \frac{V_m}{2^{n_{dpwm}}} \tag{A3.15}$$

APPENDIX 4

Conducted emission test CE03 of MIL STD 461C

A4.1. Purpose

The purpose of the test is to measure conducted emission on DC power input leads of test samples which connect externally or interface with other equipment that are not part of the test sample

A4.2. Specification limit

CEO3 specification limit is shown in Figure A4.1. Both narrowband and broadband conducted emissions in the frequency range 15 kHz to 50 MHz must not exceed the limits shown in Figure A4.1.

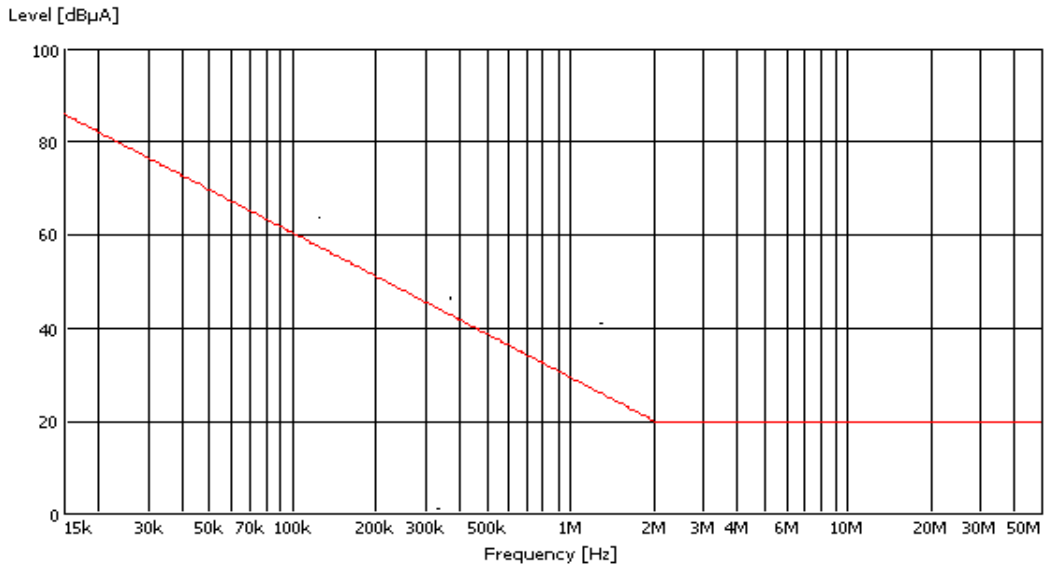

Figure A4.1: MIL-STD –461C Limit for conducted emission CE03 narrow band

A4.3. Test procedure

Test setup is shown in Figure A4.2. The EMI emission measurement system is located in the antechamber. Test sample is kept on the test stand in the anechoic chamber. The test sample is powered. The current probe, singer Model 91550-1B, that covers the frequency range of 15 kHz to 50 MHz is clamped on to the positive

or return DC line close to the feed through capacitor. The output of the current probe is connected to the EMI emission measurement system and the output of the EMI test measurement system is given to plotter. Appropriate plots covering the frequency range are taken. As the specification limits are also plotted on the same plot, the emission level can be easily compared with those specification limits. The specification limit settings on the emission measurement system may be chosen as per the system operational manual. The equipment used are 1) EMI Test Receiver R & S ESU 20 Hz to 26.5 GHz. 2) Current probe singer model 91550-1B (NM 17/27)

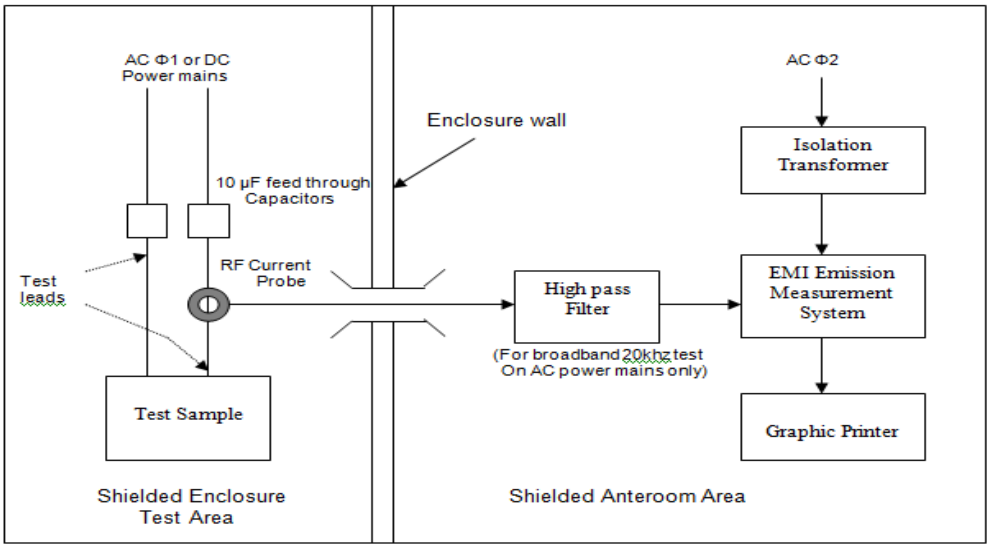

Figure A4.2: Test set up foe CE03 power lead measurements

LIST OF PAPERS BASED ON THESIS

Papers in refereed international journals

Published

1. Sajitha G, N. Selvaganesan and Thomas Kurian, “Method to eliminate the limit cycle oscillation for digitally controlled DC-DC converter using reduced state Kalman Filter”, IET Power Electronics, vol. 9, Issue 12, pp. 2445-2452, Oct. 2016.

2. Sajitha G and Thomas Kurian, “Reduction in limit cycle oscillation and conducted electromagnetic emissions by switching frequency adjustment in digitally controlled DC-DC Converters”, European journal of Power Electronics and Drives, vol. 26, Issue 3, pp. 96-103, 2016.